Design Project

VLSI Design

Instructor: **Dr. Tassadaq Hussain**

Course Code: EE437

Semester: Spring 2024

Credit Hours: 3+1

Project Statement:

Develop a Convolution Filter in Verilog HDL for image filtration. The digital system of the convolution filter takes inputs:

a) Image with a size of 128x128 bytes (grayscale).
b) 3x3 and 9x9 bit filter to perform 2D convolution on the input image and store the values in output memory.
c) The inputs can be stored in a user-defined local memory (BRAM) using RS232 and USB interface.
d) The output should be linked with a VGA controller.

Deliverables: The project deliverables include:

a) Iverilog and GTKWave simulation report.
b) Verilator simulation report.
c) FPGA Implementation
d) OpenLane GDS File Results.

By working on this project, students will be able to apply real-time implementation of digital logic design approaches and understand RTL to GDS concepts. They will also develop skills in designing and implementing a complete digital system using Verilog Hardware Description Language (HDL) and gain hands-on experience with FPGA and ASIC technology.

Marking Scheme:

Total Marks: 100

1. **HDL code** : 35

2. **GTK-wave Simulation and FPGA prototyping results with detailed report**: 25

3. ASIC (OpenLane/OpenRoad) Design Compiler Results: 30

4. **Presentation** : 10

Characteristics of CEP:

Course Name	**WK**	**PLO (WA)**	**WP**	**Blooms Taxonomy Level**
VLSI	WK2	PLO2, PLO3, PLO4, PLO7	WP3: Depth of knowledge required,	P1, C2, C1