Riphah International University

Faculty of Engineering & Applied Sciences

B.Sc. Electrical Engineering

Spring 2019

Complex Engineering Problem

Course: VLSI Design **Duration: 6 weeks**

Assignment Date:_____ **Marks: _100_**

Question: **Design a standard ASIC chip for heart rate identification using ECG signals in an Intel 65 nm process and the activity factor is 0.4, neglect wire capacitance:**

1) Design logic circuit using switch level design approach on **Modelsim Simulation** tool and **Xilinx ISE Design Compiler.**
2) Calculate the maximum operating frequency of the chip.
3) Measure power of the chip.
4) Implement its layout using VLSI design approach.

Attained CEP Attributes:

1. Preamble
2. Range of conflicting requirements
3. Depth of analysis required
4. Depth of knowledge required
5. Interdependence