Field Programmable Analog Arrays: A Brief History

Summary:

Due to the rapid change of communication standards, ASICs re-designing and development are very expensive. Therefore, there is an increasing need of reconfigurable analog circuits. Field programmable analog array (FPAA) is the solution.

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Introduction

Sensor-readout interfaces and filters in transceiver front-ends for wireless communication are implemented in the analog domain. Although analog circuits are very complicated and hard to design, they are very power efficient. For this reason, analog circuits are suitable for mobile applications. Usually, these analog circuits are application specific integrated circuits (ASICs).

Due to the rapid change of communication standards, ASICs re-designing and development are very expensive. Therefore, there is an increasing need of reconfigurable analog circuits. Field programmable analog array (FPAA) is the solution.

FPAAs are flexible integrated devices containing several configurable analog blocks (CABs) and signal routing network between them. By programming the CABs and changing the connections between them, various analog functions could be implemented. The main purpose of FPAAs is the rapid-prototyping of analog circuits like there digital counterpart the field programmable gate array (FPGA). Unlike FPGAs, FPAAs are more application driven than being a general purpose; this is because analog circuits are more complex, non-linear, noisy and difficult to design than digital circuits.

In conclusion, the main purpose of designing FPAAs is the need of adaptive analog circuits in low power analog front-ends. Moreover, FPAAs are needed for rapid-prototyping of analog circuitry to ensure the correct functionality of mixed signal system where simulations are not enough.

History

Since the term was first used in 1991 by Lee and Gulak [1], the FPAA shown in Figure 1 has become an interesting widely research topic. It was introduced to describe the basic idea of CABs which can be connected by a routing network, and are configured digitally. The idea was further enhanced by the same authors in 1992 and 1995 [2, 3] where op-amps, capacitors, and resistors can be connected to form a biquad, for instance. The chip was manufactured in a 1.2µm CMOS technology, and operates in the 20 kHz range at a power consumption of 80 mW.

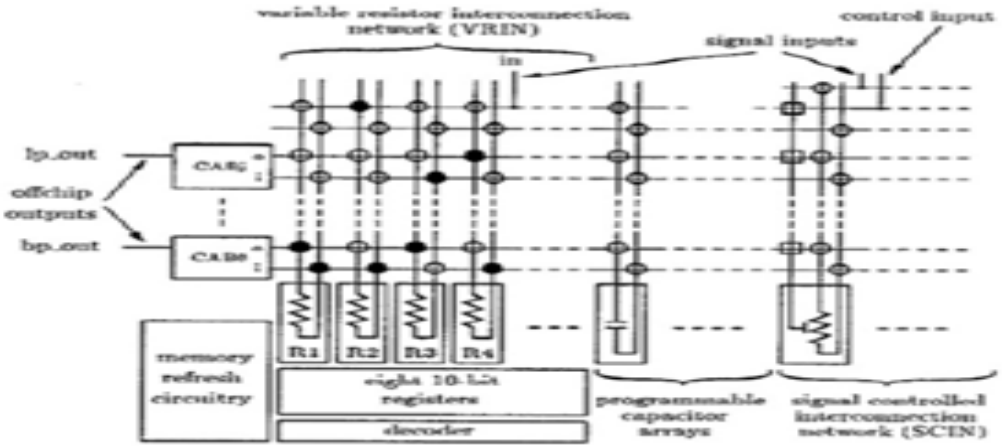

Figure 1 FPAA system architecture by Lee and Gulak [1]

In 1995, a similar idea, the electronically-programmable analog circuit (EPAC) was presented by Pierzchala et al. [4]. Although their test chip featured only a single integrator, they nonetheless proposed the concept of a local interconnect architecture to avoid the bandwidth limiting switches in a routing network, and the design was commercialized.

A successful commercial FPAA supplier is Anadigm [5] whose products allow simple instantiations of complex filters, but the switched capacitor (SC) technique limits their bandwidth to 2 MHz.

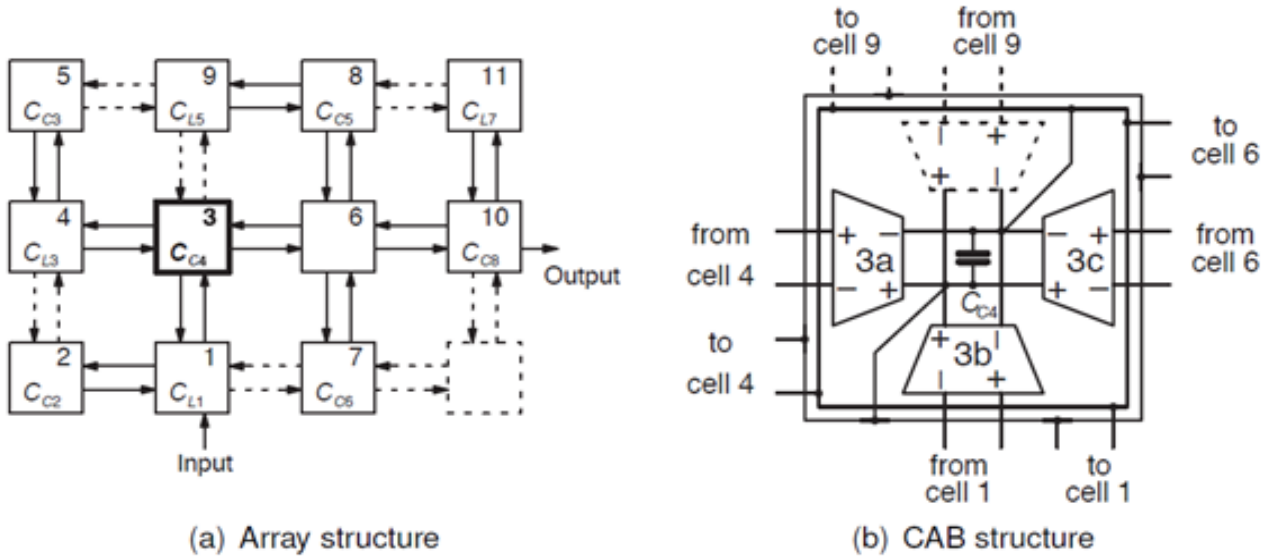

Figure 2 Schematic of Chessboard connection scheme by Pierzchala [6]

In 2002, a continuous-time (CT) FPAA using programmable operational transconductance amplifiers (OTAs) and programmable capacitor arrays was presented by Pankiewicz et al. [6] that functioned in the 1 MHz range. The FPAA was designed in a chessboard layout shown in Figure 2 with local interconnects and switches and the OTA tuning is achieved by a programmable current mirror. This technique allows Gm tuning with 5-bit precision which is limited by the large chip area each additional bit of precision adds. Therefore, this technique is not feasible for high precision tuning in an FPAA due to the chip area it would require.

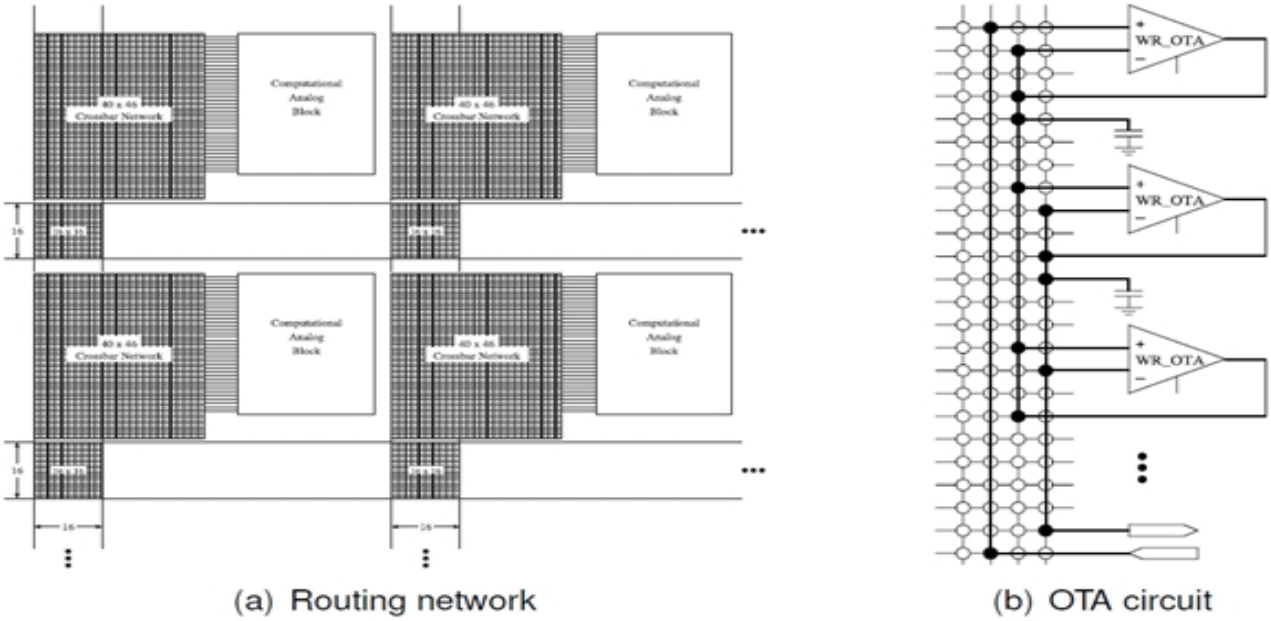

Figure 3 FPAA architecture of RASP

Also in 2002, the reconfigurable analog signal processor (RASP) shown in Figure 3 was presented by Hall et al. [7]. In 2005, a second version of the RASP followed [8]. Both implement a classic layout with CABs connected with a global routing network. Floating gates are used as switches in the routing network and in tuning the active elements. The design attempts to achieve the complexity and flexibility similar to that of FPGAs by incorporating high-level elements such as second order bandpass filters and four-by-four vector-matrix multipliers into its CABs. This makes interesting applications easily possible such as Fourier analysis, but degrades its frequency performance. The 0.35 µm CMOS technology used and the necessary large routing network – which introduces many bandwidth-limiting switches into the signal path – limit its frequency range to around 100 kHz. The programming of the floating gates is controlled externally by a PCB containing an FPGA and analog switches; the chip itself is not able of independent reconfiguration.

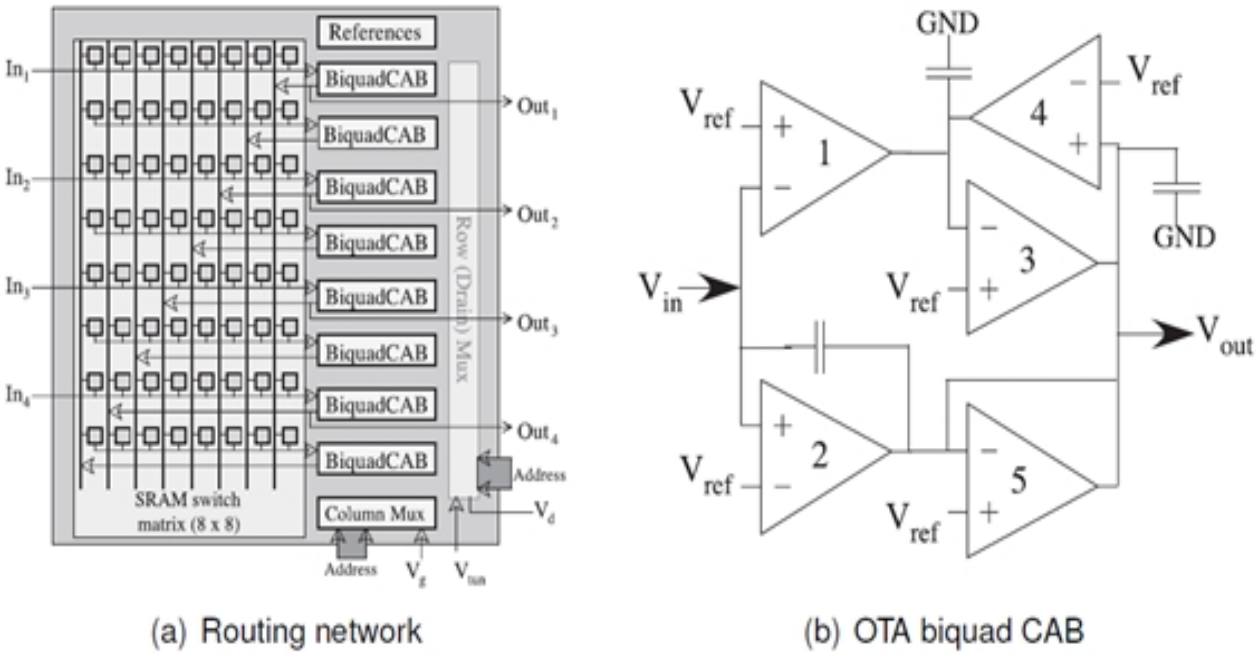

Figure 4 FPAA based on biquad tunable by floating gates [9]

In 2007, the above group introduced a specialized version of the RASP [9]. The complex CABs are all replaced by simpler CABs each containing just one second-order biquad tunable by floating gates shown in Figure 4. They are still connected by a classic global routing network using floating gate switches. The maximum achievable bandwidth is improved to around 10-15MHz on the expense of its reduced complexity and application range. The OTAs are operated in sub-threshold region by floating gates.

In parallel with the above work, the parallel connection of OTAs (Figure 5) to achieve tuning was proposed by Pavan and Tsividis [10] in 2000. The overall transconductance of the amplifier depends

linearly on the number of OTAs switched on. This allows wide range tuning without the usual drawbacks, e.g. low dynamic range at low frequency settings. This

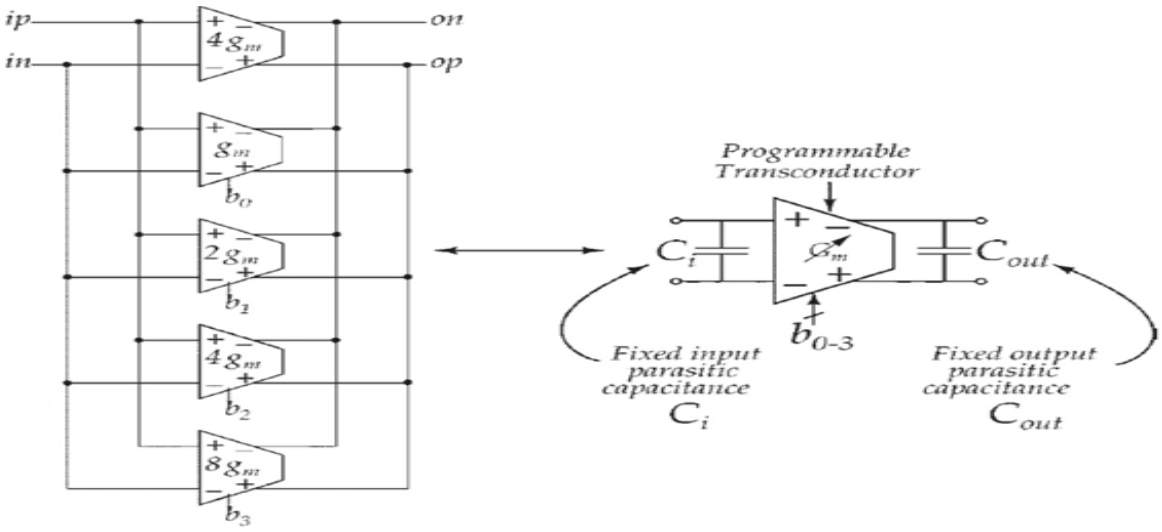

Figure 5 Parallel OTA connection proposed by Pavan at el.

technique was taken up and developed by Joachim Becker in 2004 [11] when he proposed its use in a hexagonal local interconnect architecture.

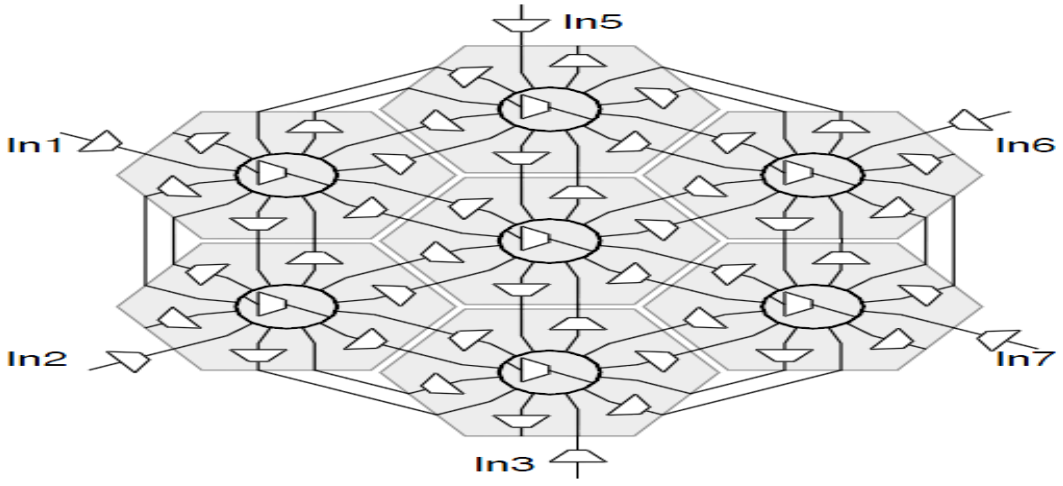

Figure 6 Hexagonal FPAA structure

It does not require a routing network and eliminates switching in the signal path which improves the frequency response. Instead, the tunable Gm cell consisting of parallel connected OTAs is used to

implement the required Gm-C stages and to implement the routing at the same time. By simply switching all of a cells parallel connected OTAs off, a signal path is cut off. The arrangement of the cells in a hexagonal lattice as shown in Figure 6 allows the instantiations of filters of all orders. By doubling the OTAs in a tunable Gm cell, and connecting half of them with inverted output terminals, the signal can be transconducted either direct or inverted, depending on which set of OTAs is switched on.

In 2005, Fabian Henrici joined the work group and developed a novel switchable and invertible OTA which cut the number of OTAs in a tunable Gm cell by half, thus reducing parasitic capacitances and nearly doubling the maximum FPAA bandwidth. Together with Joachim Becker, he developed an FPAA using his OTA and the local interconnect architecture introduced by Becker. This collaboration resulted in the first manufactured and published FPAA in 0.13µm CMOS technology, which was presented at ISSCC (International Solid States Conference) in 2008 [12]. Moreover, Henrici continued on this work and manufactured an FPAA chip in 0.13µm CMOS technology with continuous tuning through floating gates.