Lab13
Simple Hardware Design Lab: MicroBlaze

RIPHAH INTERNATIONAL UNIVERSITY

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Introduction

This lab guides you through the process of using Xilinx Platform Studio (XPS) to create a simple processor system. An MHS file and design netlists will be created.

Objectives

After completing this lab, you will be able to:

- Create an XPS Project by using Base System Builder (BSB)
- Create a simple hardware design by using Xilinx IPs available in the Embedded Design Kit

Procedure

The purpose of the lab exercises is to walk you through a complete hardware and software processor system design. Each lab will build upon the previous lab. The following diagram represents the completed design.

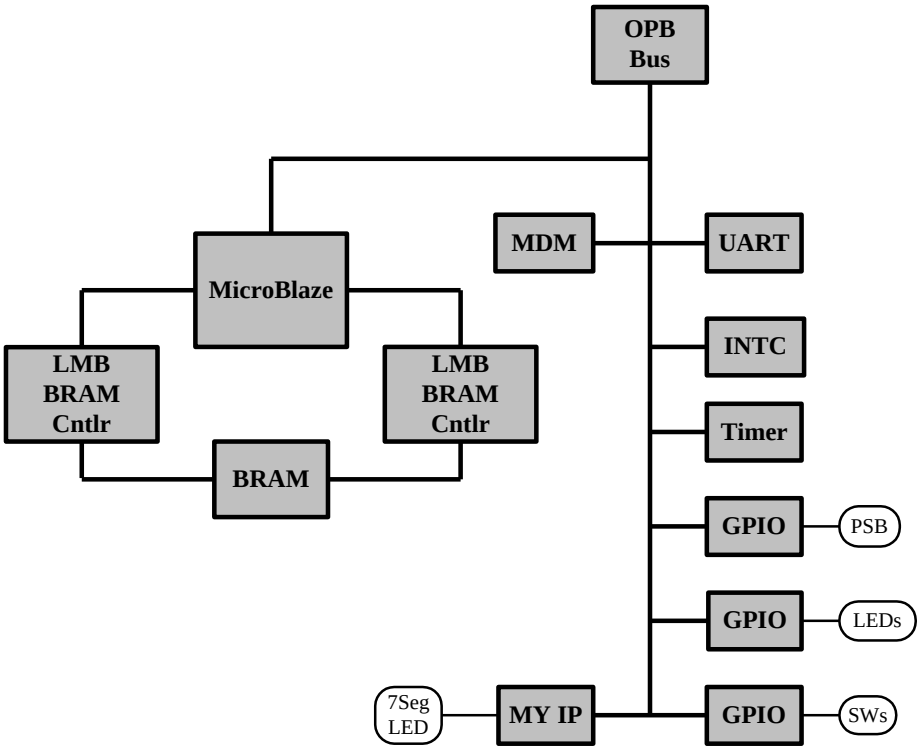


Figure 2c-1.Completed Design

In this lab, you will use the BSB of the XPS system to create a processor system consisting of the following processor IP:

- *MicroBlaze*
- *LMB BRAM controllers for BRAM*
- *BRAM*
- *OPB bus*
- *OPB MDM*
- *OPB UART*
- *OPB GPIO for Push Buttons*
- *OPB GPIO for LEDs*

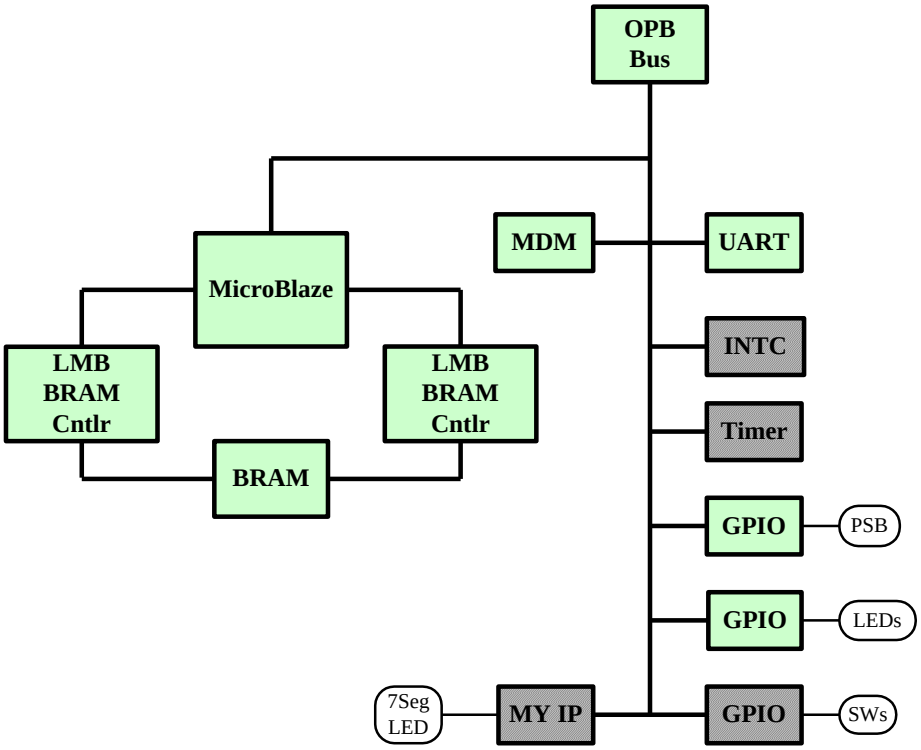


Figure 2c-2. Processor IP

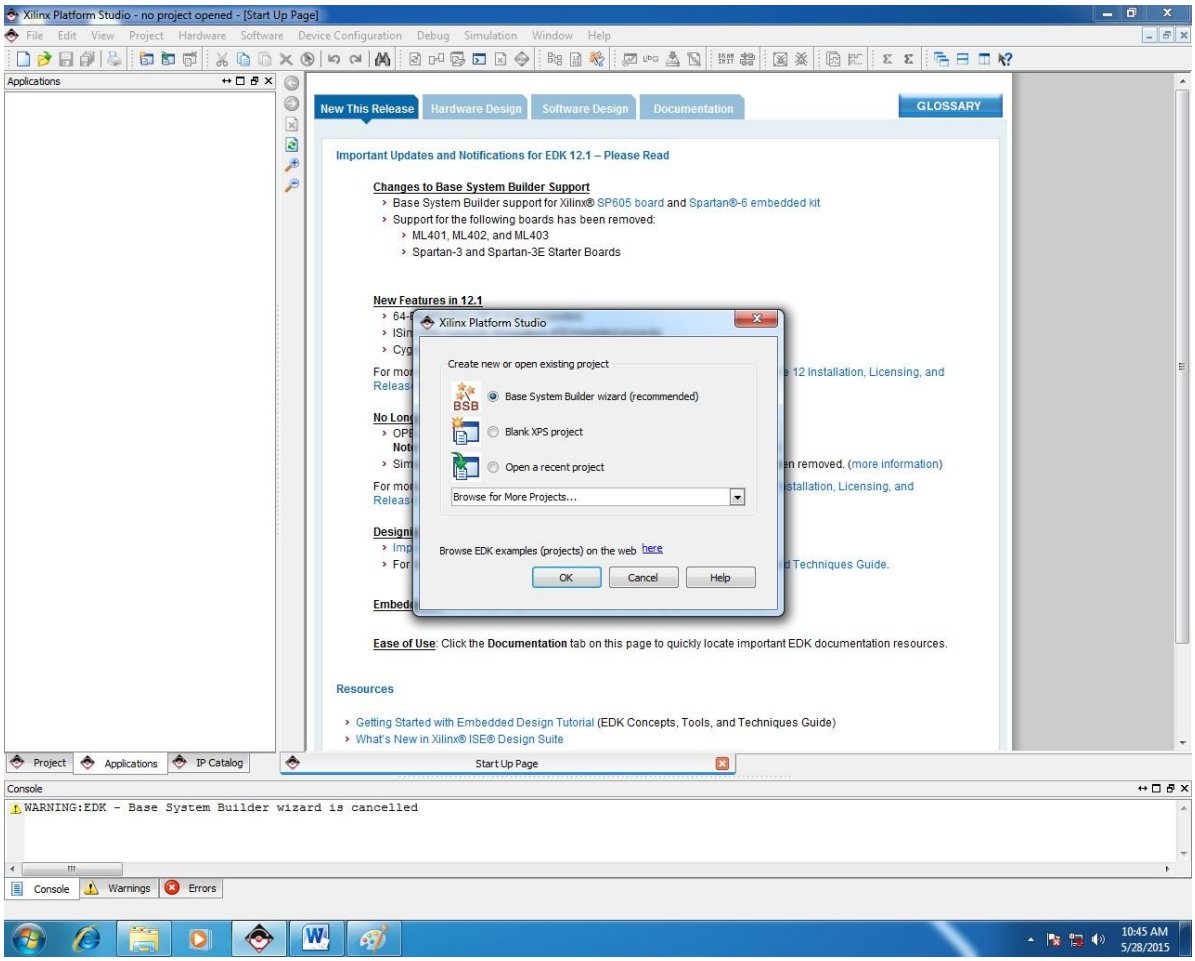
This lab comprises three primary steps: you will create a project using the Base System Builder, analyze the project created, and generate the processor system netlists. Below each general instruction for a given procedure, you will find accompanying step-by-step directions and illustrated figures providing more detail for performing the general instruction. If you feel confident about a specific instruction, feel free to skip the step-by-step directions and move on to the next general instruction in the procedure.

Opening the Project Step 1

Launch Xilinx Platform Studio (XPS) and create a project file in c**:\xup\embedded\labs\lab1mb** by using Base System Builder. Select MicroBlaze as the processor, the processor clock frequency as 50 MHz, the bus clock frequency as 50 MHz, and On-chip H/W debug module as the debug interface.

❶ Open XPS by clicking **Start → Programs → Xilinx Platform Studio 6.2i → Xilinx Platform Studio**

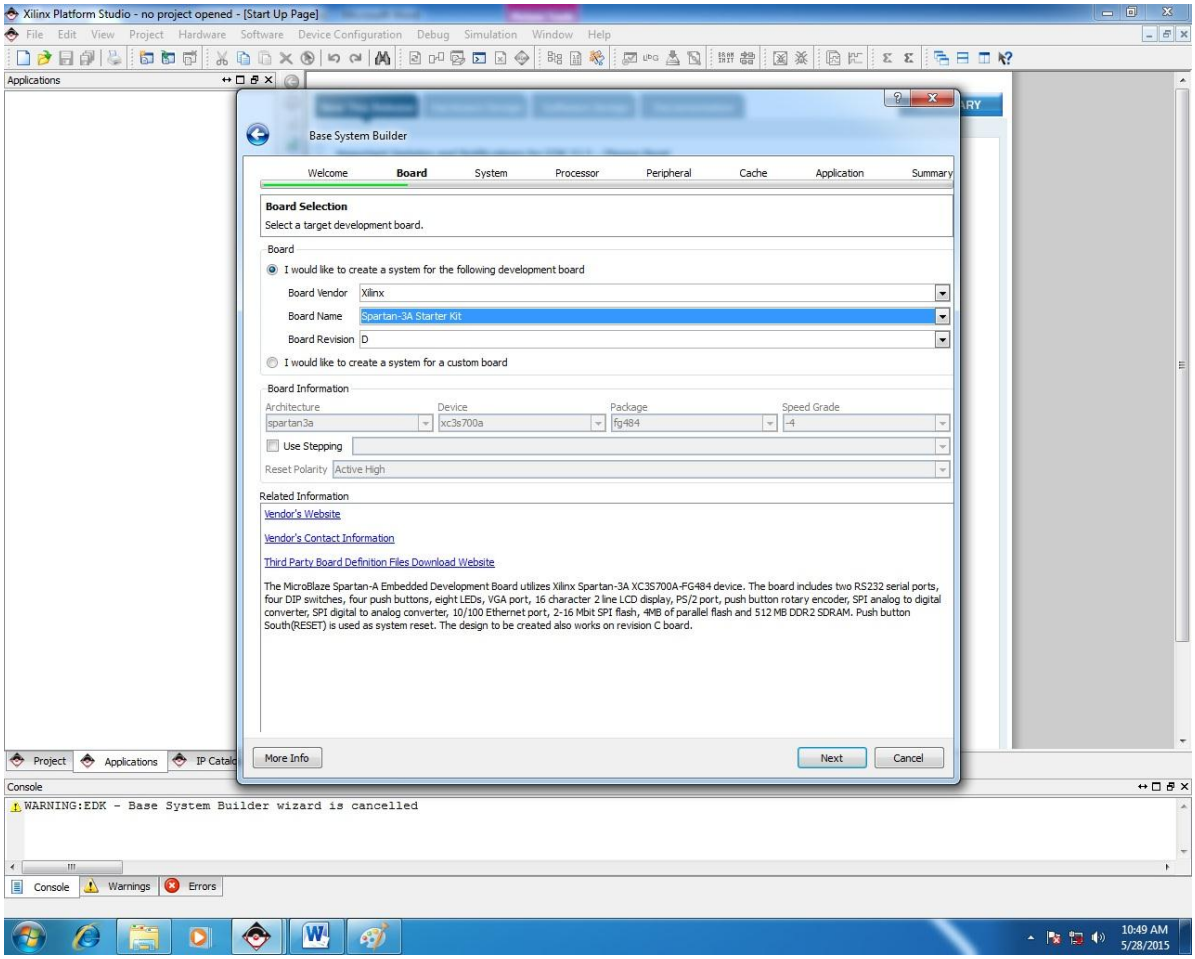
❷ Click **File → New Project → Base System Builder**



New Base System Builder Wizard Project Dialog

- Specify the **Project File** as c**:\xup\embedded\labs\lab1mb\system.xmp**
- Keep the **Peripheral Repository Directory** check box **unchecked**

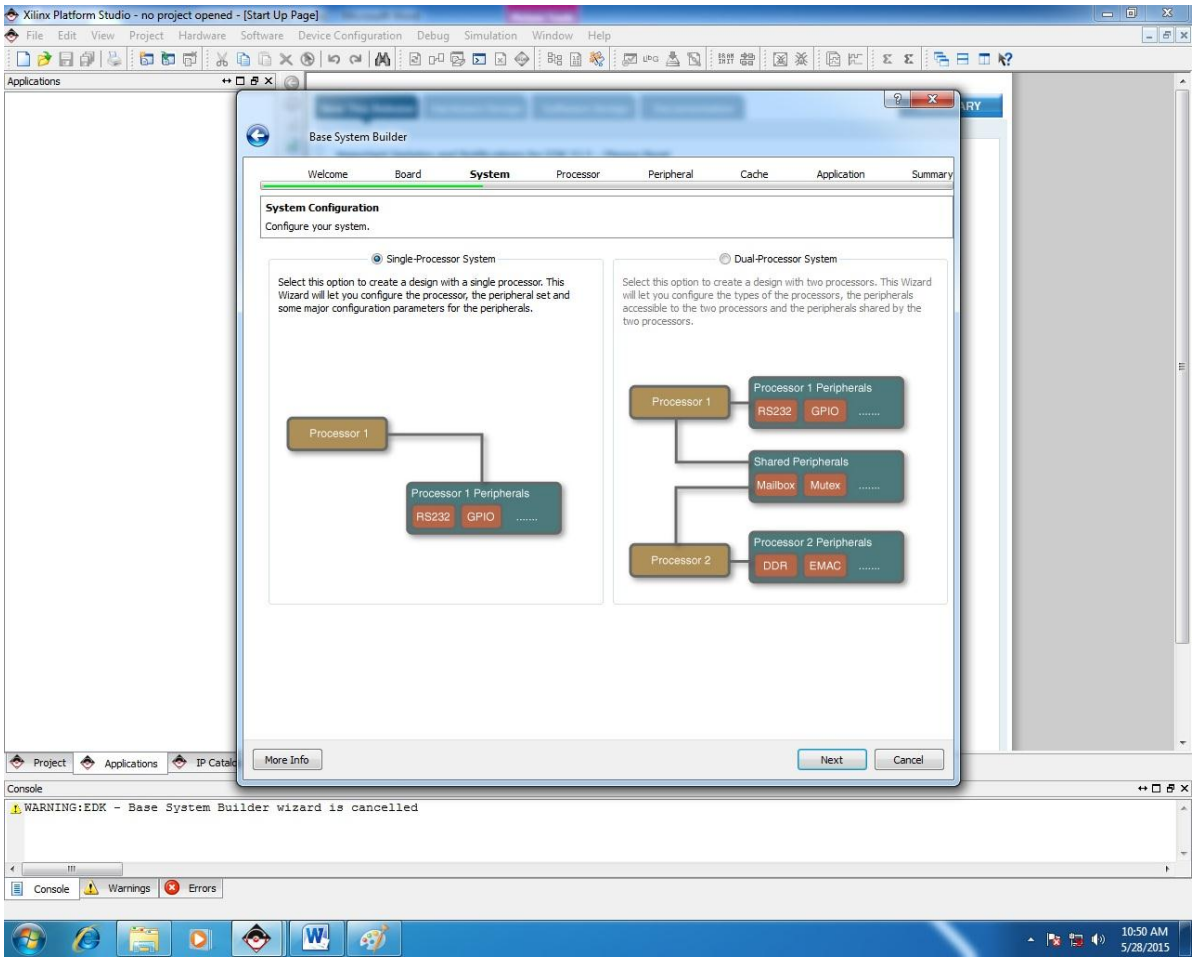
❸ Click **OK** and you will see the **Select Board** dialog box



Select Board Dialog

- Specify **Xilinx** as the **Board Vendor**
- Select **Spartan-3 Starter Board** as the **Board Name**
- Select **E** as the **Board Revision**

❹ Click the **Next** button and the **Selection Processor** dialog will be displayed

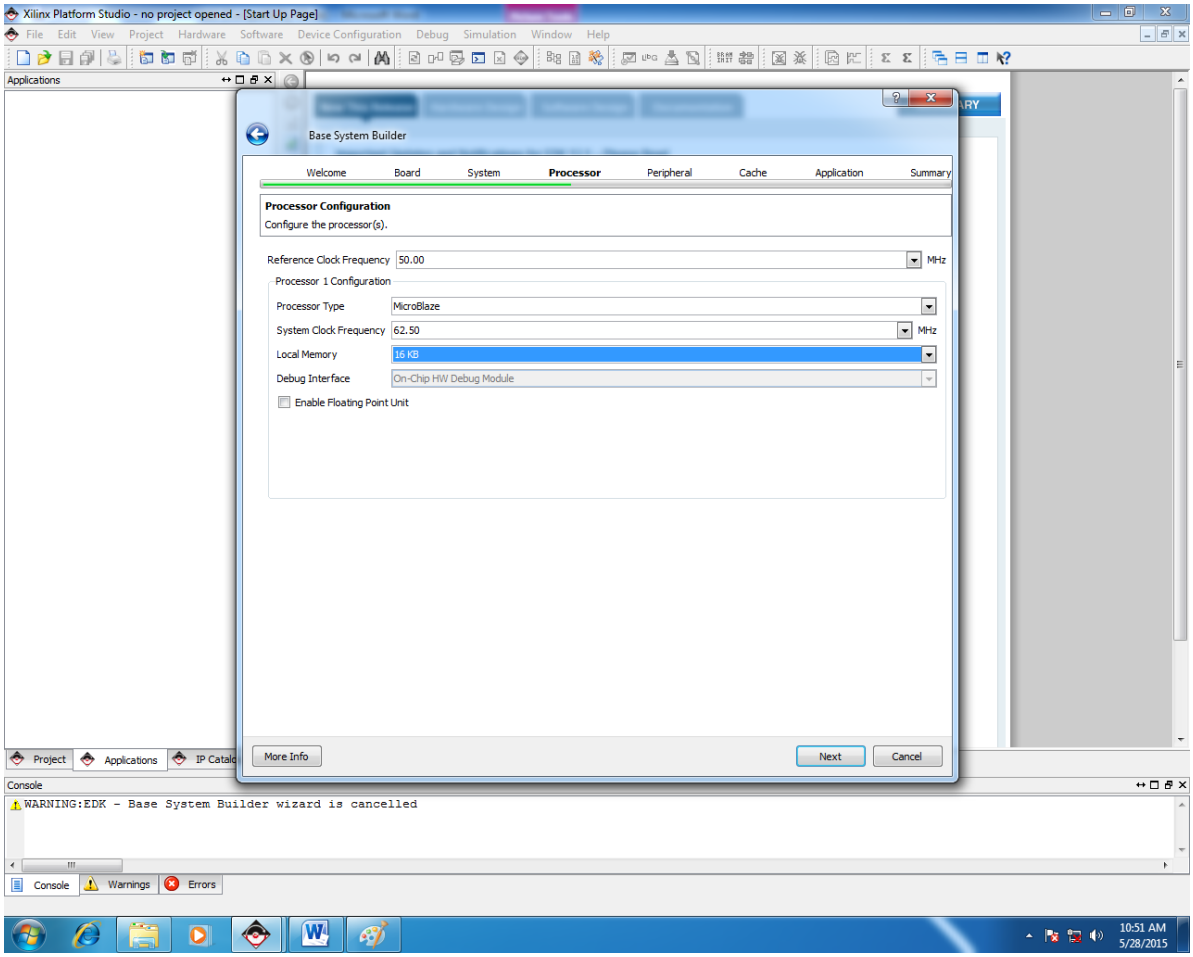


. Select Processor Dialog

❺ Select **MicroBlaze** as the processor

❻ Click the **Next** button and the **Configure Processor** dialog will be displayed. Select settings to match the following:

- **Processor Clock Frequency: 50 MHz**
- **Debug Interface: On-chip H/W debug module**
- **Local Data and Instruction Memory: 8 KB**
- **Cache Enabled:** unchecked

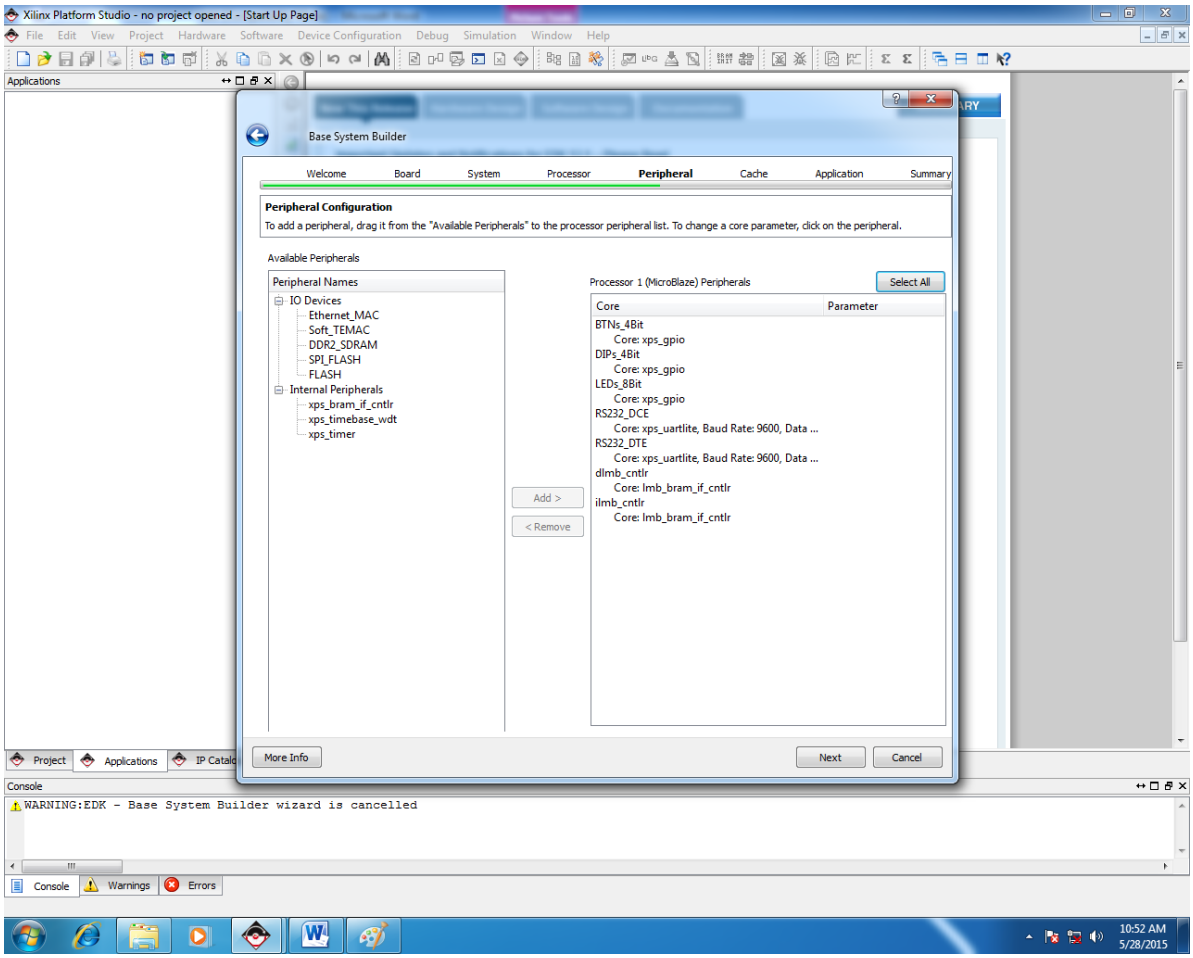


Configure Processor Dialog

Select **RS232**, **LEDs_8Bit**, and **Push_Buttons_3Bit** as the only external devices and generate the linker script.

❶ Click **Next** and the **Configure IO Interfaces** dialog will be displayed. Uncheck the **LED_7SEGMENT** and **DIP_Switches_8Bit** boxes, leaving the remaining devices with the default settings

Note: *Depending on your screen resolution settings, the* **Configure IO Interfaces** *may show more or less devices in the initial screen than the one shown below.*



Configure IO Interfaces Dialog

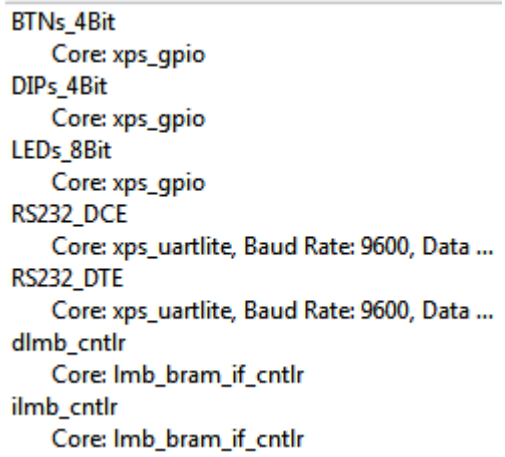
❷ Click the **Next** button and the **Configure Additional IO Interfaces** dialog will appear

Note: *Depending on your screen resolution settings, the* **Configure Additional IO Interfaces** *may show more or less devices than in the figure below, and the IO device may be displayed in a different position.*

Configure Additional IO Interfaces Dialog

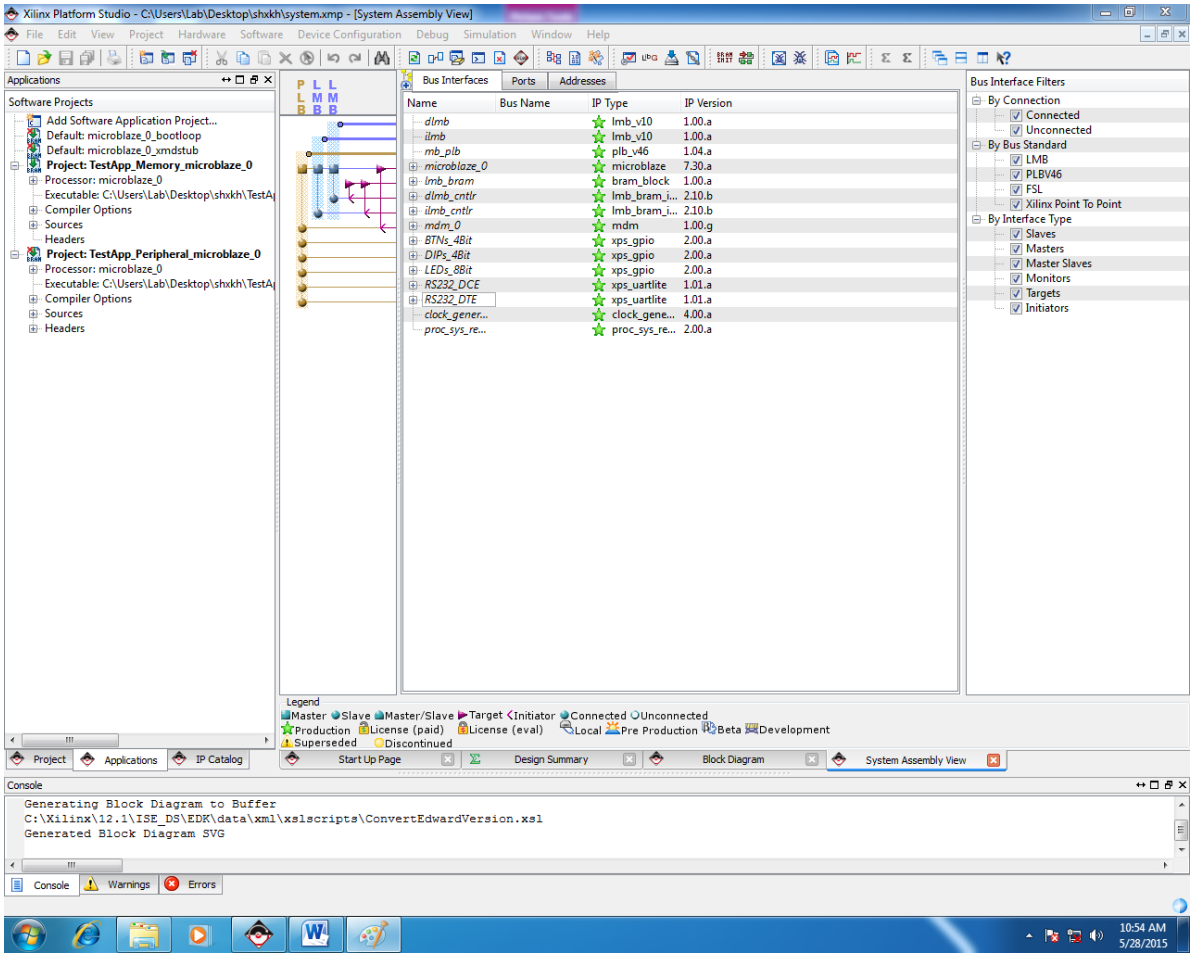
❸ Uncheck the **SRAM_256Kx32** box

❹ Click the **Next** button and the **Add Internal Peripherals** dialog will appear



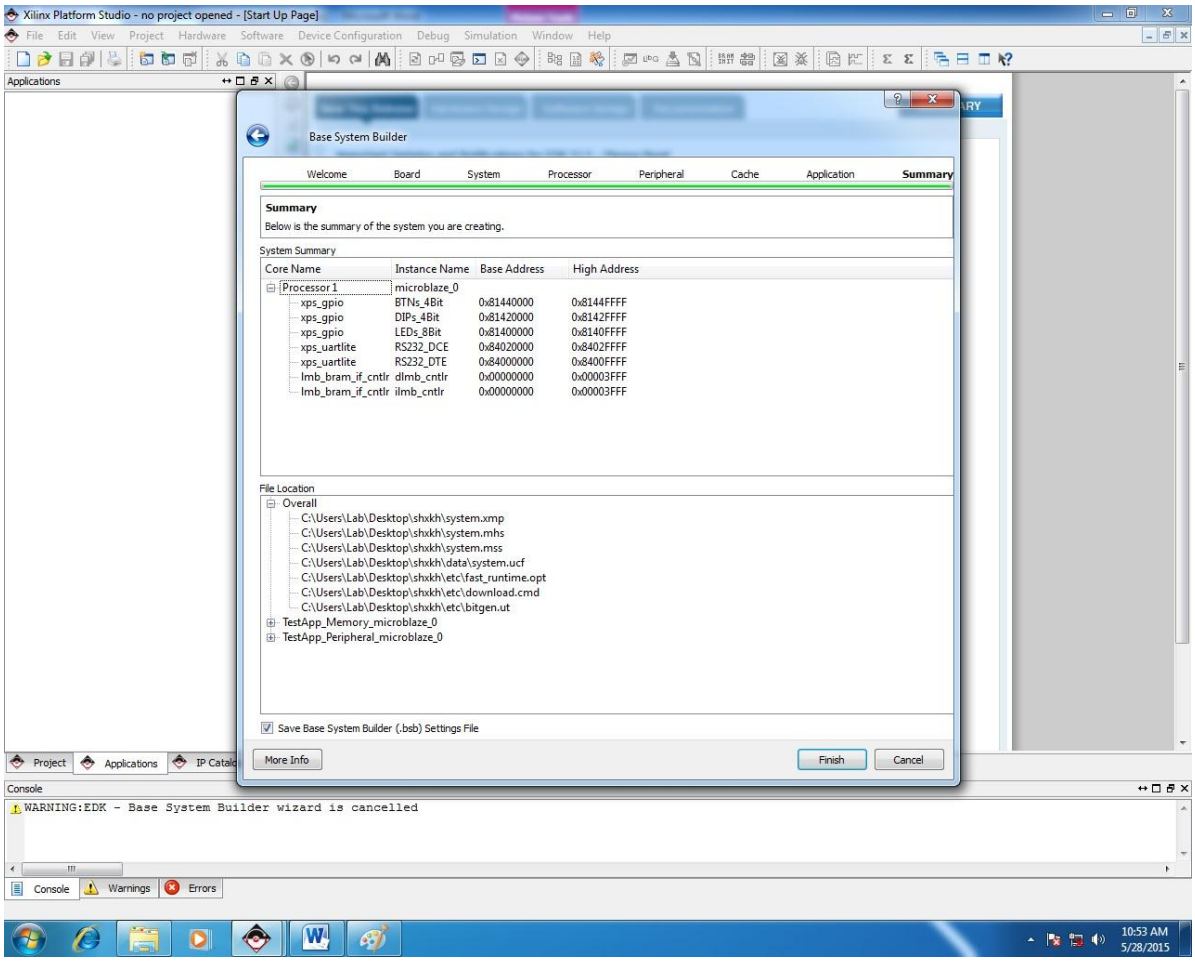
Add Internal Peripherals Dialog

❺ Click the **Next** button and the **Software Configuration** dialog box will appear



Software Configuration Dialog

❻ Click the **Next** button and the **System Created** dialog will appear (summary of the system being created)



System Created Dialog

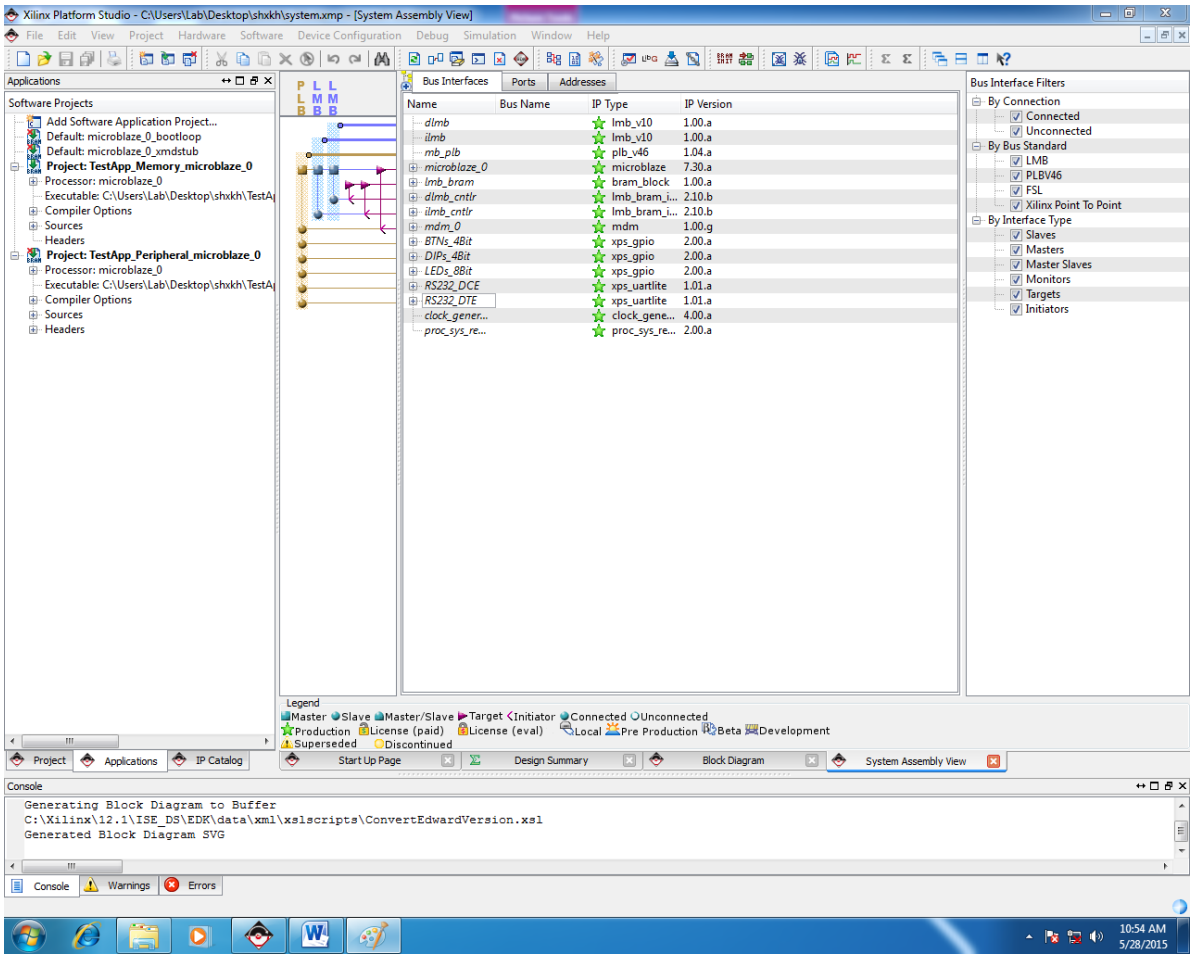
❼ Click the **Generate** button

❽ A congratulations screen will appear, indicating the files the BSB has created. Click the **Finish** button to finish generating the project

Analyzing the Created Project Step 2

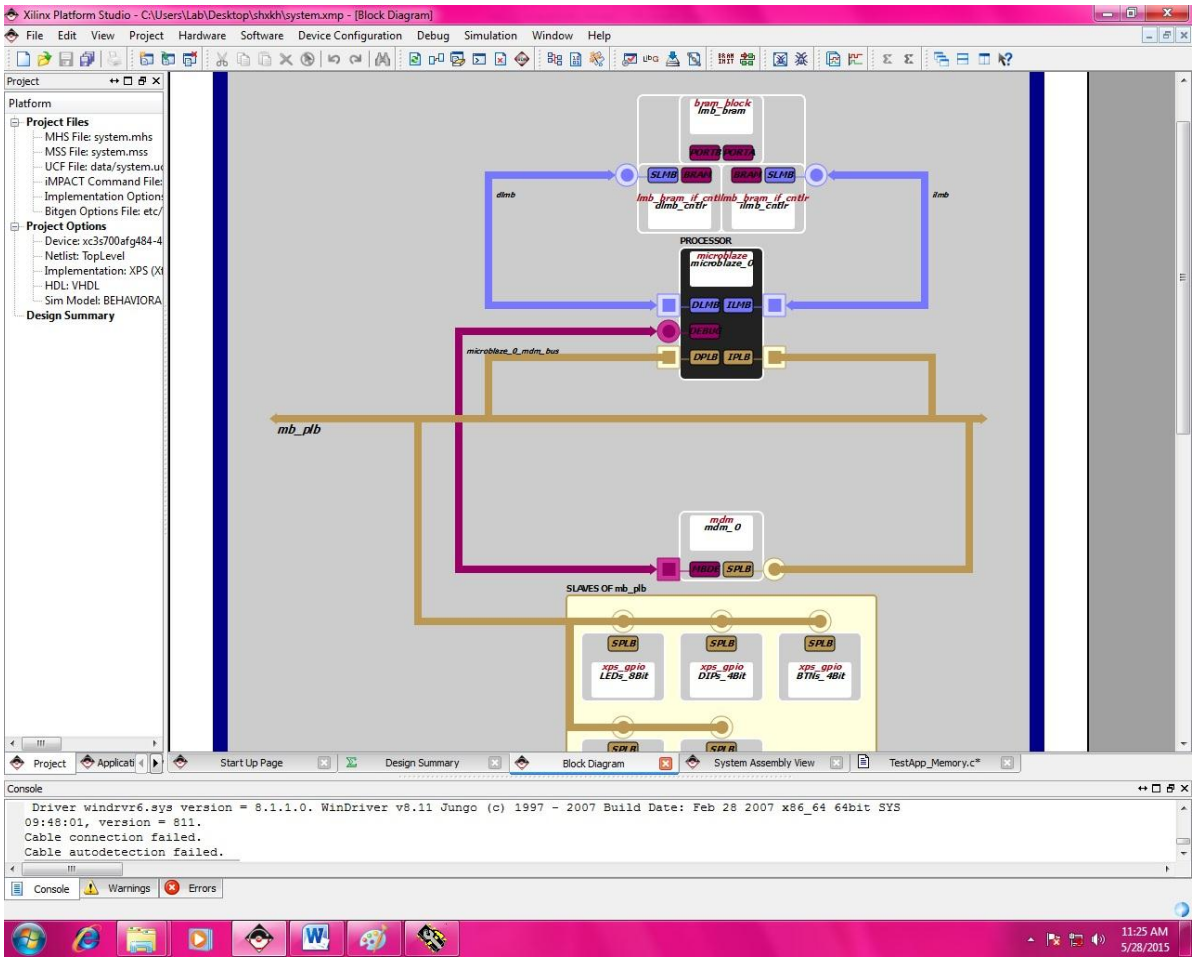
Using the **System** tab, study the project files created, view the project in schematic view, and practice editing the schematic view

❶ In the XPS **System** tab, double-click the **system.pbd** file under **Project Files** to open a schematic view



Selecting the Schematic File

❷ Observe the various components that are used in the design



Schematic View of the Generated Project

You will see MicroBlaze™ connected to the ilmb, dlmb, and mb_opb buses as well as the lmb_bram_contlrs. Notice that the opb_mdm and three instances of the opb_gpio components are connected to the OPB bus.

1. Double-click the opb_uartlite block, go through the various fields, and answer the following questions.

Instance name:	RS232
Base address:	0x80002100
High address:	0x800021ff
Explicit parameter value for C_BAUDRATE:	9600
Explicit parameter value for C_CLK_FREQ:	MHz
Number of interrupt pins:	0

2. Double-click the top opb_gpio block, go through the various fields, and answer the following questions.

Instance name: _____
Base address: _____
High address: _____
Explicit parameter value for C_ALL_INPUTS: _____
Explicit parameter value for C_GPIO_WIDTH: _____
Number of interrupt pins: _____

3. Double-click the bottom opb_gpio block, go through the various fields, and answer the following questions.

Instance name: _____
Base address: _____
High address: _____
Explicit parameter value for C_ALL_INPUTS: _____
Explicit parameter value for C_GPIO_WIDTH: _____
Number of interrupt pins: _____

Notice that you can change the parameters (such as base address, address range, or C_ALL_INPUTS) here to reflect the design specifications.

❸ Select the top **gpio** and drag it to the left of the **OPB** bus

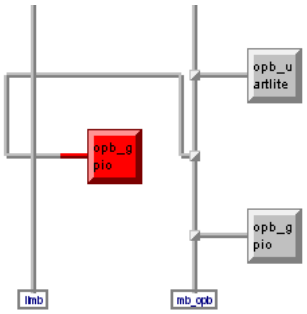


Figure 2c-15. Moving an Instance in a Schematic

❹ Double-click the **opb_gpio** instance which you just moved. An **object properties** form will open

❺ Select **Symbol** in the object properties form

❻ Select the **SOPB** pin in the right window and click the **Remove** button

❼ In the **Pins on Symbol** (right) window, choose the **Right** direction

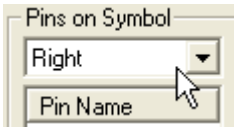


Figure 2c-16. Assigning pins on the Appropriate Edge of a Symbol

❽ Select the **SOPB** pin under the **Available Pins** and click the **Add** button

❾ Click the **Apply** button and you will observe that the connection to the bus has changed

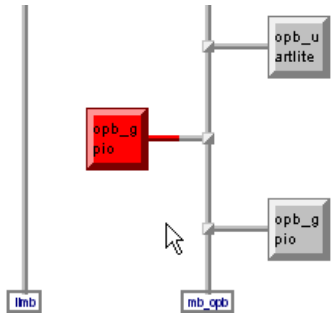


Figure 2c-17. Move and Rewire Instance

❿ Close the schematic without saving the changes

Generating the Hardware Netlists Step 3

Using the **PlatGen** utility, generate the hardware netlist

❶ In XPS, click **Tools → Generate Netlist** or click  in the toolbar

Observe the netlist generation in the console window as it progresses.

❷ Open **Windows Explorer** and click **Start → Programs → Accessories → Windows Explorer**

❸ Browse to the project directory (Lab1mb). Several directories containing VHDL wrappers and implementation netlists have been created

4. List the directories.

Generating the FPGA bitfile Step 4

Using the **ISE** tools, generate the FPGA bitfile.

❶ In XPS, click **Tools → Generate Bitstream** or click  in the toolbar

Observe the netlist generation in the console window as it progresses.

❷ Open **Windows Explorer** and click **Start → Programs → Accessories → Windows Explorer**

❸ Browse to the project directory (Lab1mb). No new directories have been created. Look in the implementation directory. The

5. What is the name of the bit file in the implementation directory

_____

_____

Conclusion

The BSB can be used in XPS to create a project. Several files, including an MHS file representing the processor system and a PBD file representing the schematic view, are created. Once the system has been defined, the netlist of the processor system can be created. In a future lab in this course, you will learn how to add other cores and simulate the design.