# Lab13 Simple Hardware Design Lab: MicroBlaze



# Simple Hardware Design Lab: MicroBlaze

# Introduction

This lab guides you through the process of using Xilinx Platform Studio (XPS) to create a simple processor system. An MHS file and design netlists will be created.

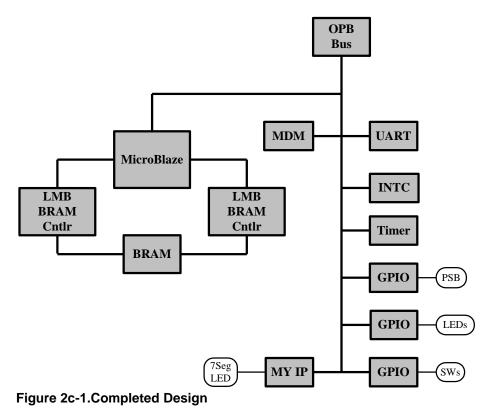
# **Objectives**

After completing this lab, you will be able to:

- Create an XPS Project by using Base System Builder (BSB)
- Create a simple hardware design by using Xilinx IPs available in the Embedded Design Kit

# **Procedure**

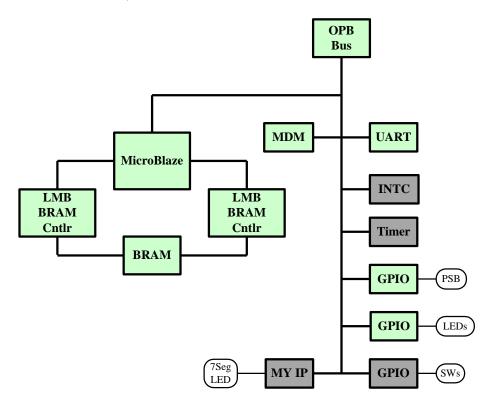
The purpose of the lab exercises is to walk you through a complete hardware and software processor system design. Each lab will build upon the previous lab. The following diagram represents the completed design.





In this lab, you will use the BSB of the XPS system to create a processor system consisting of the following processor IP:

- MicroBlaze
- LMB BRAM controllers for BRAM
- BRAM
- OPB bus
- OPB MDM
- OPB UART
- OPB GPIO for Push Buttons
- OPB GPIO for LEDs



### Figure 2c-2. Processor IP

This lab comprises three primary steps: you will create a project using the Base System Builder, analyze the project created, and generate the processor system netlists. Below each general instruction for a given procedure, you will find accompanying step-by-step directions and illustrated figures providing more detail for performing the general instruction. If you feel confident about a specific instruction, feel free to skip the step-by-step directions and move on to the next general instruction in the procedure.

## **Opening the Project**



Simple Hardware Design Lab: MicroBlaze



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Step 1

Launch Xilinx Platform Studio (XPS) and create a project file in c:\xup\embedded\labs\lab1mb by using Base System Builder. Select MicroBlaze as the processor, the processor clock frequency as 50 MHz, the bus clock frequency as 50 MHz, and On-chip H/W debug module as the debug interface.

• Open XPS by clicking Start  $\rightarrow$  Programs  $\rightarrow$  Xilinx Platform Studio 6.2i  $\rightarrow$  Xilinx Platform Studio

**⊘** Click **File** → **New Project** → **Base System Builder** 

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### New Base System Builder Wizard Project Dialog

- Specify the **Project File** as c:\xup\embedded\labs\lab1mb\system.xmp
- Keep the Peripheral Repository Directory check box unchecked



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   File Edit View Project Hardware Software Devic - 5 X +□ ₽ × @ Applications 8 X RY G Base System Builder Welcome Board Processor Peripheral Cache Application Summar System Board Selection Select a target development board. Board I would like to create a system for the following development board Board Vendor Xilinx -Board Name Spar • Board Revision D • I would like to create a system for a custom board Board Information Speed Grade Device Architecture spartan3a Package Use Stepping Reset Polarity Active High Related Information Vendor's Website Vendor's Contact Information Third Party Board Definition Files Download Website The MicroBlaze Spartan-A Embedded Development Board utilizes Xilinx Spartan-3A XC3S700A +FG484 device. The board includes two RS232 serial ports, four DIP switches, four push buttons, eight LEDs, VGA port, 16 character 2 line LCO display, PS/2 port, push button rotary encoder, SPI analog to digital converter, SPI digital to analog converter, In/100 Etheme tonto, 2-16 Mib SPI fash, 4M8 of parallel fash and 512 MB DDR2 SDRAM. Push button South(RESET) is used as system reset. The design to be created also works on revision C board. 🔶 Project 🐟 Applications 🐟 IP Catalo More Info Next Cancel ⇔⊡₽× L WARNING:EDK - Base System Builder wizard is cancelled Console
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- Click **OK** and you will see the **Select Board** dialog box

### Select Board Dialog

- Specify Xilinx as the Board Vendor
- Select Spartan-3 Starter Board as the Board Name
- Select E as the Board Revision



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• Click the **Next** button and the **Selection Processor** dialog will be displayed

. Select Processor Dialog

• Select MicroBlaze as the processor



- Click the **Next** button and the **Configure Processor** dialog will be displayed. Select settings to match the following:
  - Processor Clock Frequency: 50 MHz
  - Debug Interface: On-chip H/W debug module
  - Local Data and Instruction Memory: 8 KB
  - Cache Enabled: unchecked

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**Configure Processor Dialog** 





Select **RS232**, **LEDs\_8Bit**, and **Push\_Buttons\_3Bit** as the only external devices and generate the linker script.

• Click **Next** and the **Configure IO Interfaces** dialog will be displayed. Uncheck the **LED\_7SEGMENT** and **DIP\_Switches\_8Bit** boxes, leaving the remaining devices with the default settings

Note: Depending on your screen resolution settings, the **Configure IO Interfaces** may show more or less devices in the initial screen than the one shown below.

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### **Configure IO Interfaces Dialog**

• Click the Next button and the Configure Additional IO Interfaces dialog will appear

Note: Depending on your screen resolution settings, the **Configure Additional IO Interfaces** may show more or less devices than in the figure below, and the IO device may be displayed in a different position.

**Configure Additional IO Interfaces Dialog** 



- Uncheck the SRAM\_256Kx32 box
- Click the Next button and the Add Internal Peripherals dialog will appear

BTNs\_4Bit Core: xps\_gpio DIPs\_4Bit Core: xps\_gpio LEDs\_8Bit Core: xps\_gpio RS232\_DCE Core: xps\_uartlite, Baud Rate: 9600, Data ... RS232\_DTE Core: xps\_uartlite, Baud Rate: 9600, Data ... dImb\_cntlr Core: Imb\_bram\_if\_cntlr iImb\_cntlr Core: Imb\_bram\_if\_cntlr

Add Internal Peripherals Dialog



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• Click the Next button and the Software Configuration dialog box will appear

**Software Configuration Dialog** 



• Click the Next button and the System Created dialog will appear (summary of the system being created)

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### **System Created Dialog**

• Click the **Generate** button

• A congratulations screen will appear, indicating the files the BSB has created. Click the **Finish** button to finish generating the project

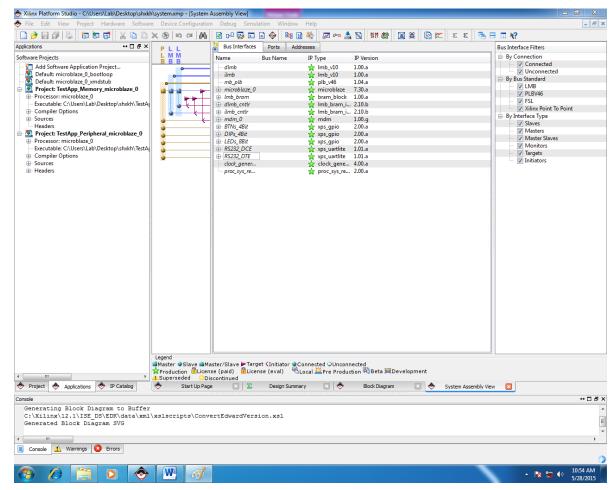


# **Analyzing the Created Project**

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Using the **System** tab, study the project files created, view the project in schematic view, and practice editing the schematic view

• In the XPS System tab, double-click the system.pbd file under Project Files to open a schematic view



Selecting the Schematic File



- 🕭 Xilinx Platform Studio CAUsers\Lab\Desktop\shxkh\system.xmp [Block Diagram] 🕭 File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help - 0 × - 5 X 🗋 🤣 🗟 🦓 😓 🐻 📷 👼 ⇔⊡ & × Project Platform bram\_block Protorm → Project Files → MHS File: system.mhs → MSS File: system.mss → UCF File: data/system.uc → iMPACT Command File: → Implementation Option: → Bridgen Options File: etc/ → Bridgen Options File: etc/ SLME bram if Bitgen Options Hile etc/
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- Observe the various components that are used in the design

Schematic View of the Generated Project

You will see MicroBlaze<sup>™</sup> connected to the ilmb, dlmb, and mb\_opb buses as well as the lmb\_bram\_contlrs. Notice that the opb\_mdm and three instances of the opb\_gpio components are connected to the OPB bus.



1. Double-click the opb\_uartlite block, go through the various fields, and answer the following questions.





2. Double-click the top opb\_gpio block, go through the various fields, and answer the following questions.

T	
Instance name:	
Base address:	
High address:	
Explicit parameter value for C_ALL_INPUTS:	
Explicit parameter value for C_GPIO_WIDTH:	
Number of interrupt pins:	

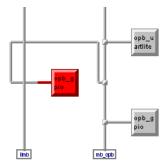


3. Double-click the bottom opb\_gpio block, go through the various fields, and answer the following questions.

Instance name:	
Base address:	
High address:	
Explicit parameter value for C_ALL_INPUTS:	
Explicit parameter value for C_GPIO_WIDTH:	
Number of interrupt pins:	

Notice that you can change the parameters (such as base address, address range, or C\_ALL\_INPUTS) here to reflect the design specifications.

• Select the top **gpio** and drag it to the left of the **OPB** bus



### Figure 2c-15. Moving an Instance in a Schematic

• Double-click the opb\_gpio instance which you just moved. An object properties form will open

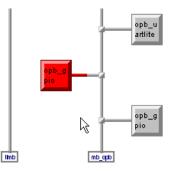
- Select **Symbol** in the object properties form
- Select the **SOPB** pin in the right window and click the **Remove** button 6
  - In the **Pins on Symbol** (right) window, choose the **Right** direction

- Pins on Symbo	ol
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### Figure 2c-16. Assigning pins on the Appropriate Edge of a Symbol

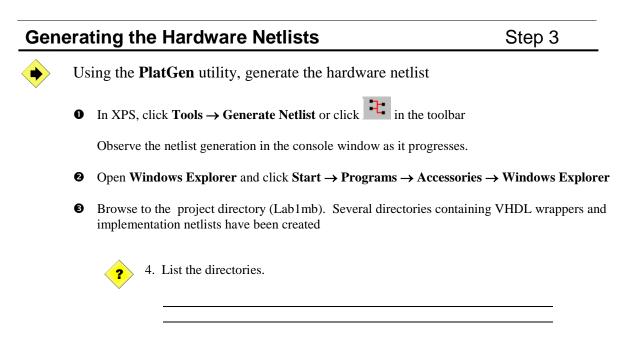


- Select the **SOPB** pin under the **Available Pins** and click the **Add** button
- Click the **Apply** button and you will observe that the connection to the bus has changed



### Figure 2c-17. Move and Rewire Instance

• Close the schematic without saving the changes





# Generating the FPGA bitfile Step 4 Using the ISE tools, generate the FPGA bitfile. In XPS, click Tools → Generate Bitstream or click In XPS, click Tools → Generate Bitstream or click Diserve the netlist generation in the console window as it progresses. Open Windows Explorer and click Start → Programs → Accessories → Windows Explorer Browse to the project directory (Lab1mb). No new directories have been created. Look in the implementation directory. The S. What is the name of the bit file in the implementation directory

# Conclusion

The BSB can be used in XPS to create a project. Several files, including an MHS file representing the processor system and a PBD file representing the schematic view, are created. Once the system has been defined, the netlist of the processor system can be created. In a future lab in this course, you will learn how to add other cores and simulate the design.

