
# VLSI Design

# Delays

Tassadaq Hussain Cheema
Professor Namal University

# Topics

Delays

Combination network delay.

Logic optimization.

# Date: Quiz 1

Name: …….. Roll Number…….....

1) If the width of a transistor increases, the current will

increase decrease not change

2) If the length of a transistor increases, the current will

increase decrease not change

3) If the supply voltage of a chip increases, the maximum transistor current will

increase decrease not change

4) If the width of a transistor increases, its gate capacitance will

increase decrease not change

5) If the length of a transistor increases, its gate capacitance will

increase decrease not change

6) If the supply voltage of a chip increases, the gate capacitance of each transistor will

increase decrease not change

# Activity

1) If the width of a transistor increases, the current will

**increase** decrease not change

2) If the length of a transistor increases, the current will

increase **decrease** not change

3) If the supply voltage of a chip increases, the maximum transistor current will

**increase** decrease not change

4) If the width of a transistor increases, its gate capacitance will

**increase** decrease not change

5) If the length of a transistor increases, its gate capacitance will

**increase** decrease not change

6) If the supply voltage of a chip increases, the gate capacitance of each transistor will

increase decrease **not change**

# Effective Resistance

Shockley models have limited value

Not accurate enough for modern transistors

Too complicated for much hand analysis

Simplification: treat transistor as resistor

Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance R

- $I_{ds} = V_{ds}/R$

R averaged across switching of digital gate

Too inaccurate to predict current at any given time

But good enough to predict RC delay

# RC Delay Model

The RC delay model is a metric used in VLSI design to calculate the signal delay between the input voltage and output voltage of the input signal.

Use equivalent circuits for MOS transistors

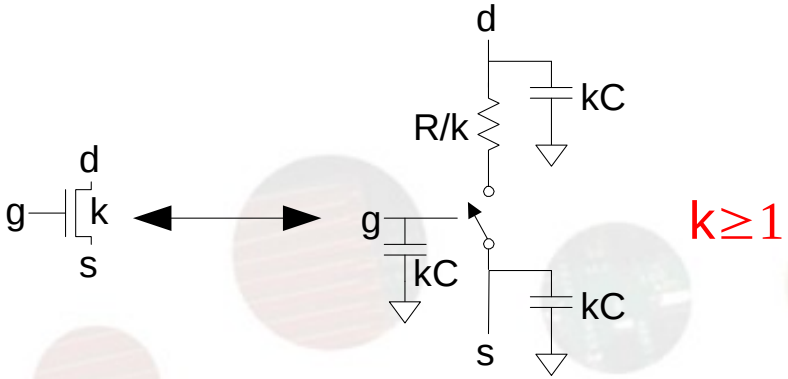
Ideal switch + capacitance and ON resistance

Unit nMOS has resistance R, capacitance C

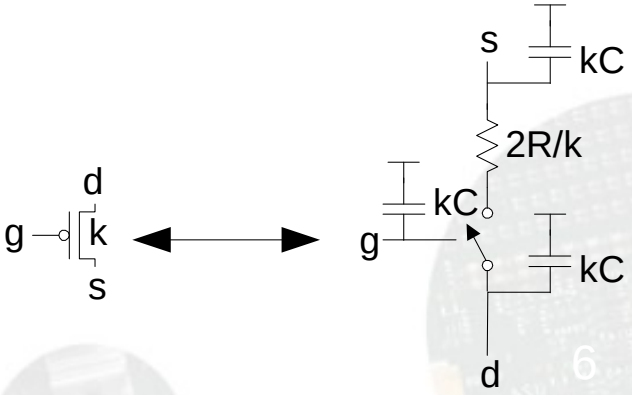
Unit pMOS has resistance 2R, capacitance C

Capacitance proportional to width

Resistance inversely proportional to width




$k \geq 1$



# RC Values

Capacitance

$C = C_g = C_s = C_d = 2$ fF/μm of gate width

Values similar across many processes

Resistance

$R \approx 6$ KΩ*μm in 0.6um process

Improves with shorter channel lengths

Unit transistors

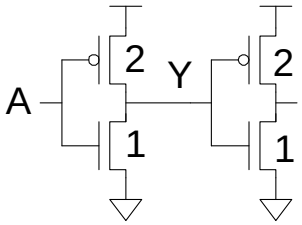
May refer to minimum contacted device (4/2 λ)

Or maybe 1 μm wide device

Doesn't matter as long as you are consistent

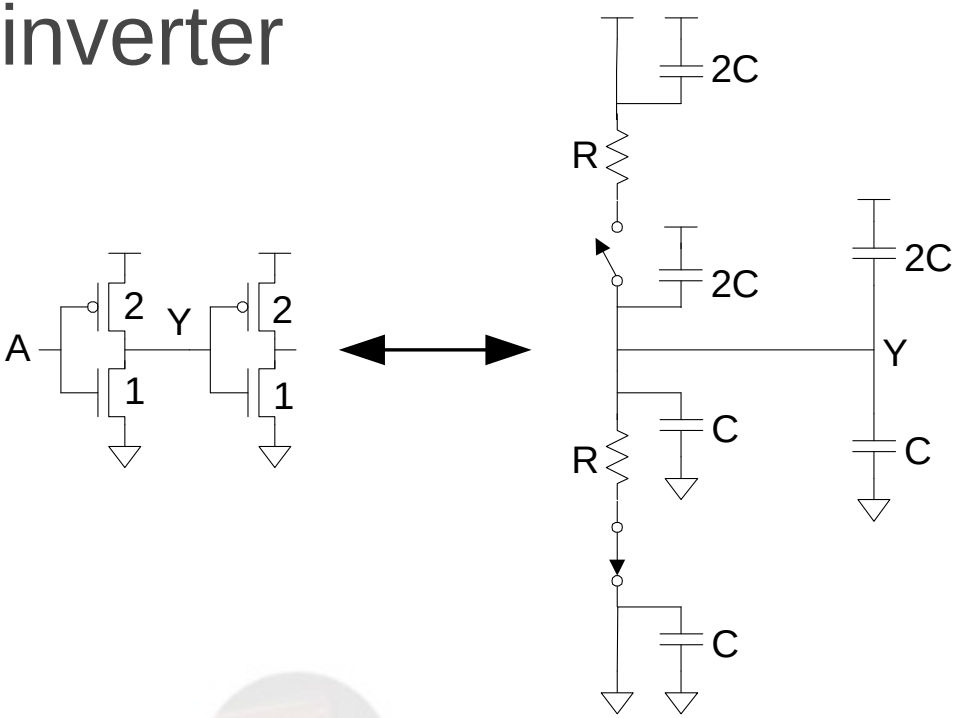
# Inverter Delay Estimate

Estimate the delay of a fanout-of-1 inverter



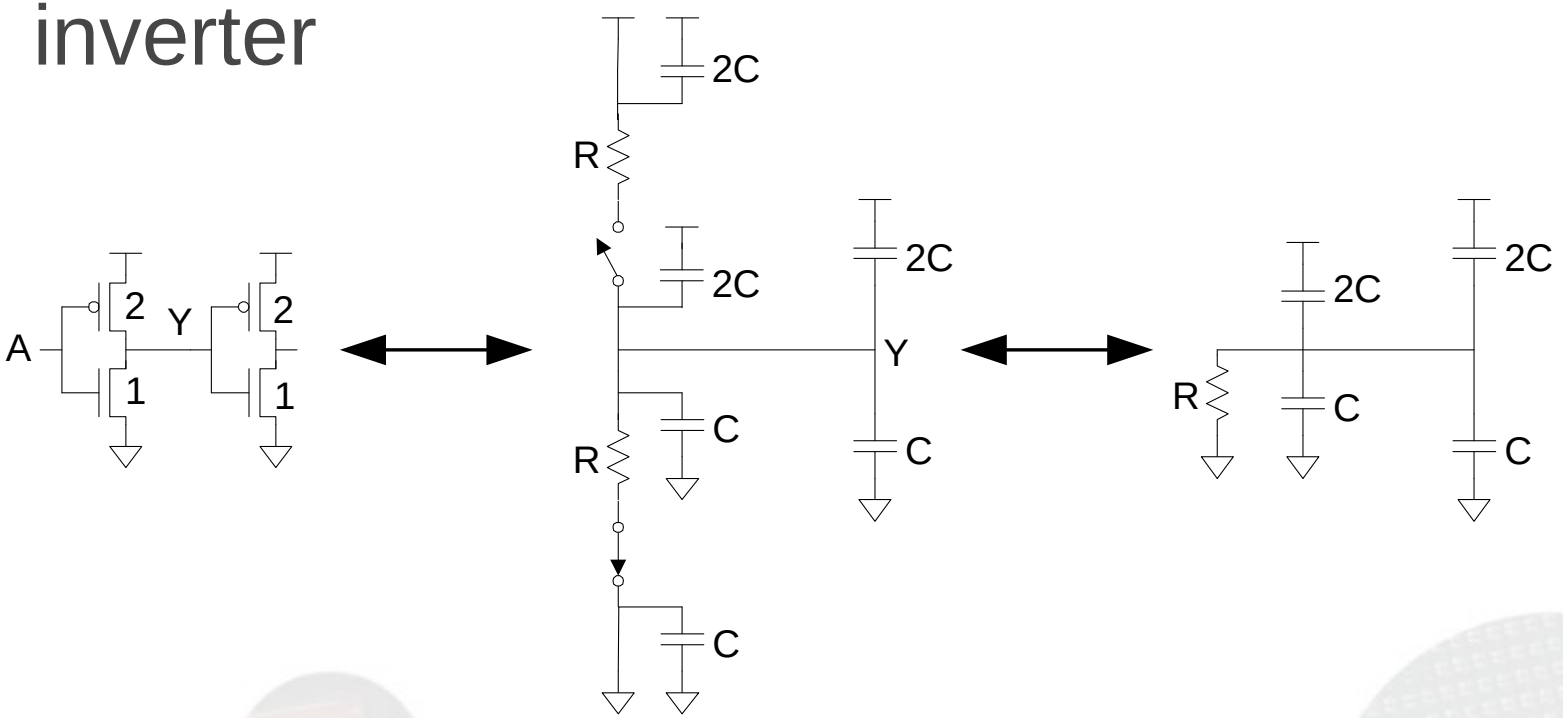
# Inverter Delay Estimate

Estimate the delay of a fanout-of-1 inverter



# Inverter Delay Estimate

Estimate the delay of a fanout-of-1 inverter



Propagation Delay

Contamination Delay

Transition Delay

Rise time

Fall time

Edge rate

Slew Rate

Skew Rate (Clock)

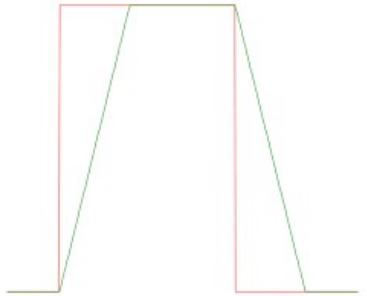
**Propagation Delay** is the amount of time it takes for a signal to travel from the input of a digital circuit to the output, after passing through any gates, buffers, or other components in the circuit. It is the time taken for the output signal to reach a stable state after the input has changed.

**Contamination Delay**, also known as the minimum delay or setup time, is the amount of time it takes for a change at the input of a digital circuit to propagate to the output of the same circuit, assuming that there are no other changes to the input during this time. In other words, it is the minimum time that the input signal must be stable before the output signal can be reliably measured.

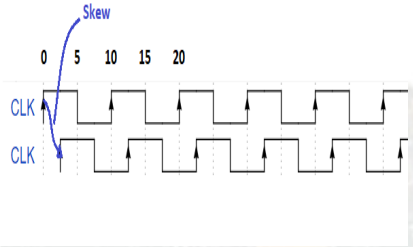
**Transition Delay**, also known as the output delay or fall time delay. This refers to the amount of time it takes for the output signal to transition from one state to another, such as from a high voltage to a low voltage. Transition delay is affected by various factors, such as the capacitance of the load connected to the output, the drive strength of the output buffer, and the characteristics of the transistors used in the circuit. It is important to consider transition delay when designing digital circuits, particularly for applications where high-speed switching is required.

Slack refers to the amount of time by which a signal's arrival can be delayed without causing a violation of the system's timing requirements. Slack is typically measured as the difference between the required arrival time of a signal and the actual arrival time of that signal, taking into account any other delays or constraints in the system.

Slew refers to the rate at which a signal changes over time. Specifically, it represents the maximum rate at which the voltage or current level of a signal can change without causing unwanted effects such as signal distortion or interference with other signals. Slew rate is typically specified in units of volts per second or amps per second, and is an important parameter to consider when designing digital systems that involve high-speed signals or analog-to-digital conversion.



Skew, on the other hand, refers to the time difference between two signals that should be synchronized or aligned in time. Skew can occur due to variations in signal propagation delays, different path lengths or routing, or variations in clock skew. Skew can cause errors in system operation, especially in systems that require precise timing synchronization between different signals or components.



# Sources of delay

- Gate delay
- Cross-talk
- Temperature
- Drive Load
- Lumped Load
- Wire
- Transmission Line

**Gate delay:** This is the time it takes for a logic gate to process an input signal and produce an output signal. It is determined by the characteristics of the gate, such as the size and type of transistors used.

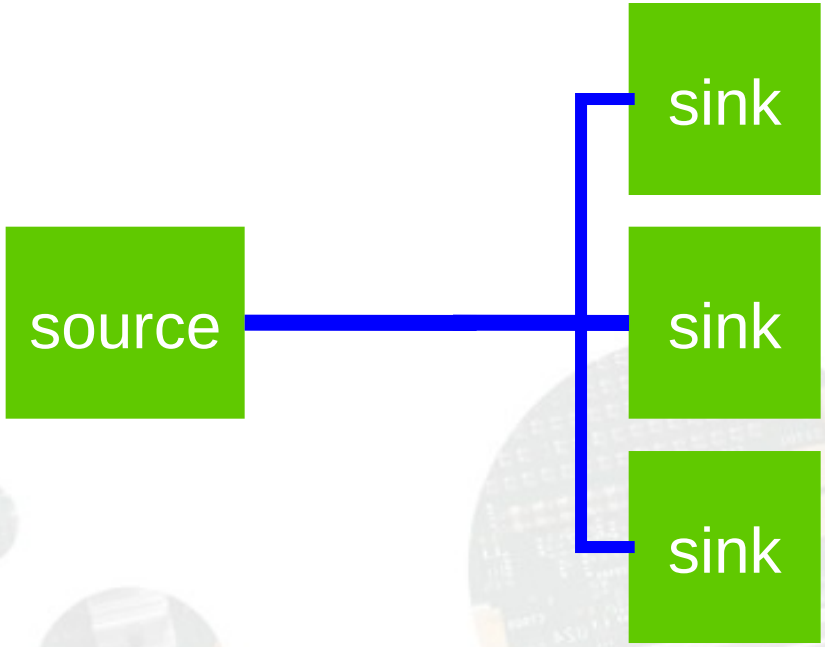
Crosstalk: When two signals running in parallel lines are too close to each other, the signals can interfere with each other, causing delays or errors.

Temperature and voltage variations: Variations in temperature or voltage can affect the performance of transistors, leading to delays or other performance issues.

# Fanout

Capacitive load: Capacitive loads, such as long wires or traces on a printed circuit board, can introduce delays due to the charging and discharging of the capacitors.

Fanout adds capacitance.

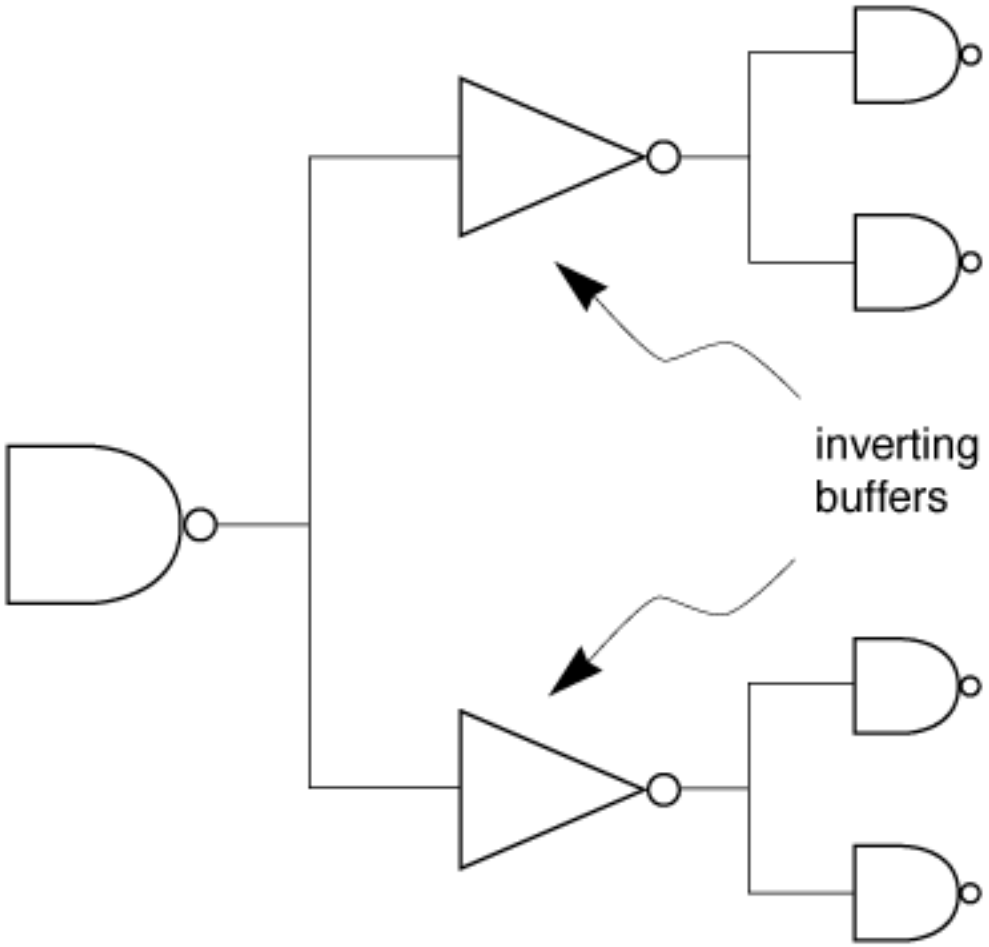


# Ways to drive large fanout

Increase sizes of driver transistors. Must take into account rules for driving large loads.

Add intermediate buffers. This may require/allow restructuring of the logic.

# Buffers

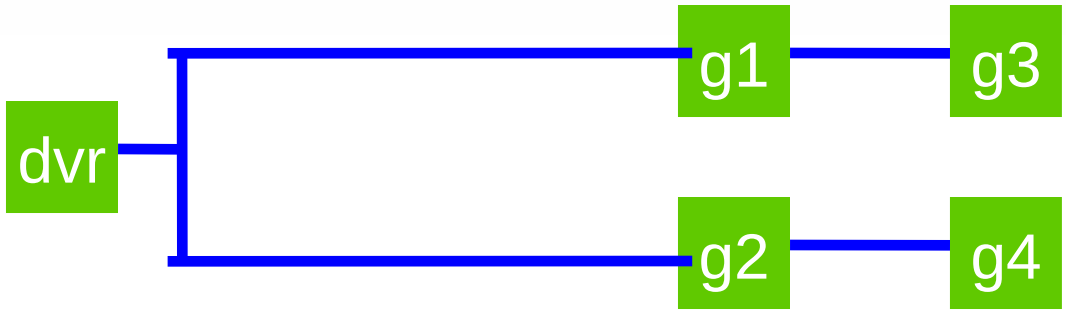


# Wire capacitance

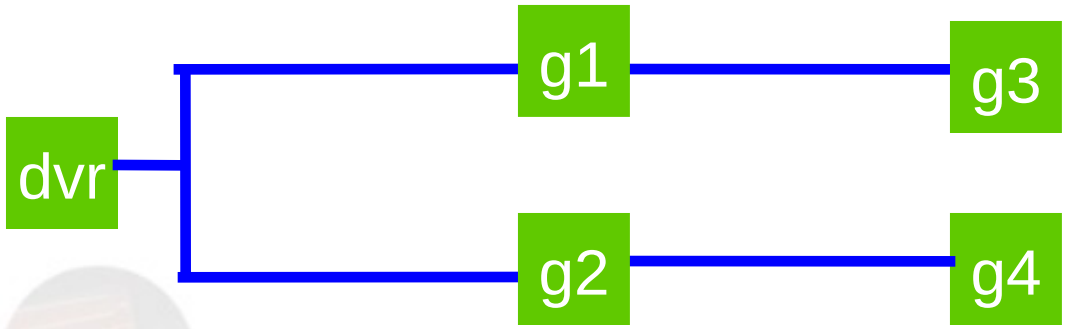
Use layers with lower capacitance.

Redesign layout to reduce length of wires with excessive delay.

# Placement and wire capacitance




unbalanced load




more balanced

# Path delay

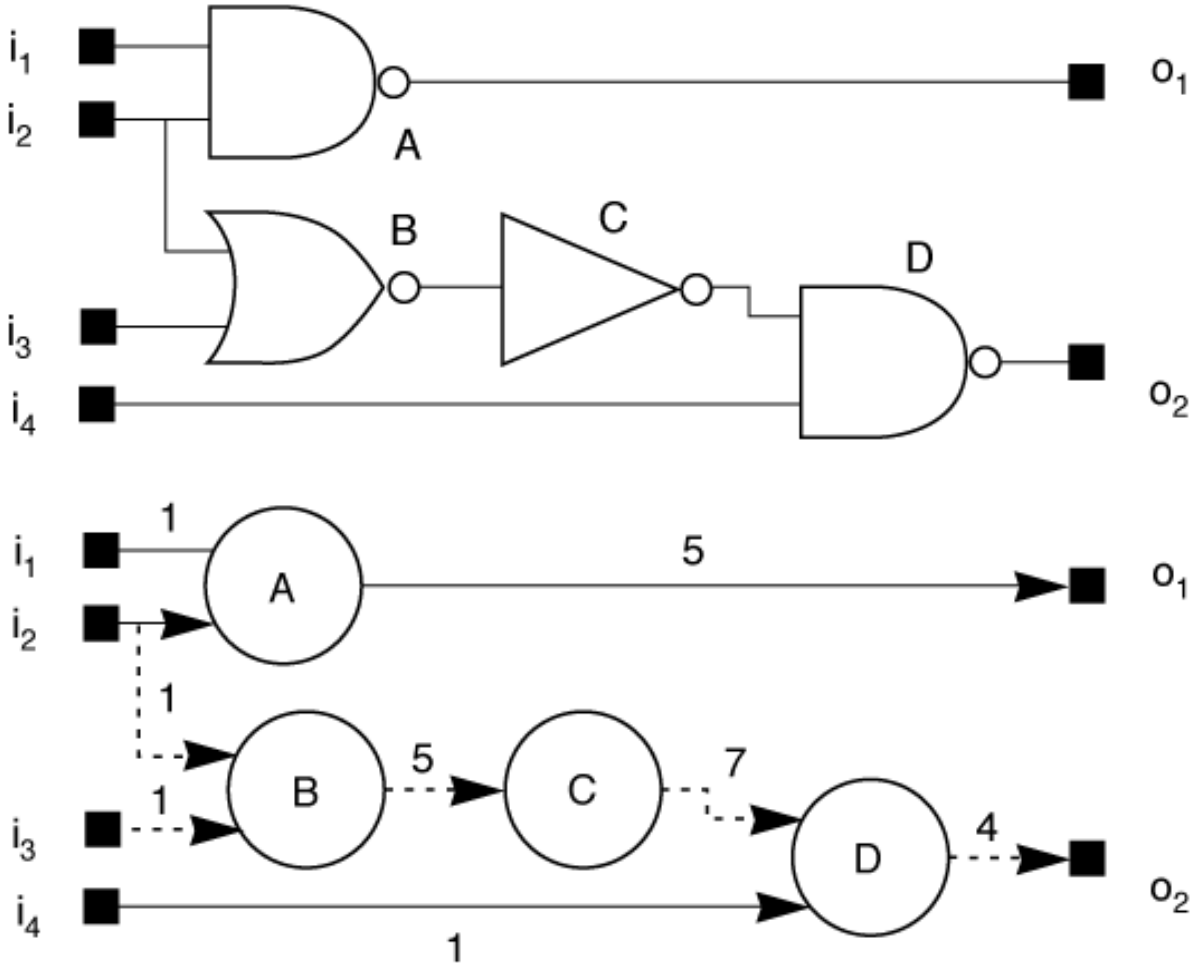
Combinational network delay is measured over paths through network.

Can trace a causality chain from inputs to worst-case output.

# Path delay example

network

graph model



# Critical path

Critical path = path which creates longest delay.

Can trace transitions which cause delays that are elements of the critical delay path.

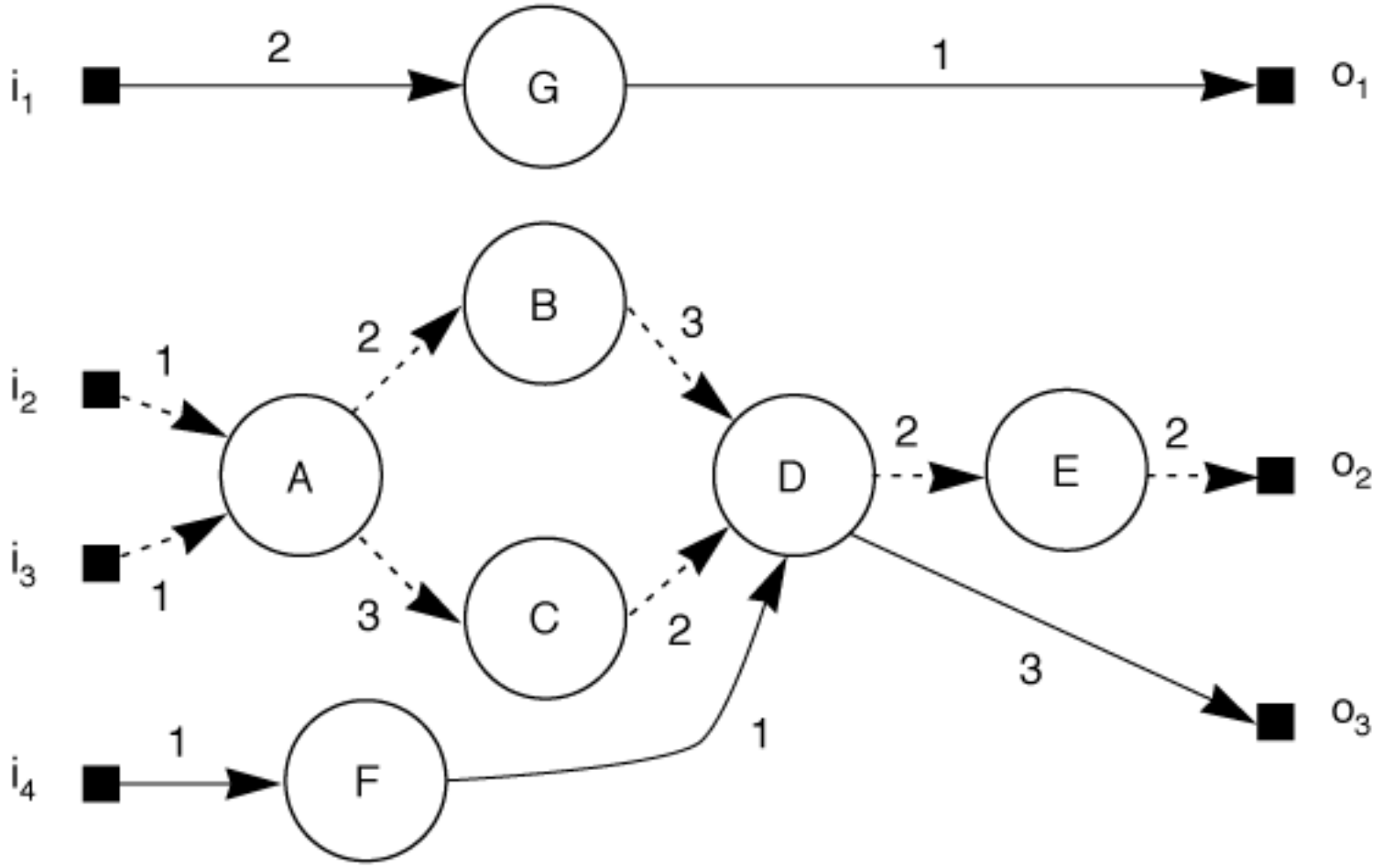
# Delay model

Nodes represent gates.

Assign delays to edges—signal may have different delay to different sinks.

Lump gate and wire delay into a single value.

# Critical path through delay graph



# Reducing critical path length

To reduce circuit delay, must speed up the critical path—reducing delay off the path doesn’t help.

There may be more than one path of the same delay. Must speed up all equivalent paths to speed up circuit.

Must speed up cut-set through critical path.

# False paths

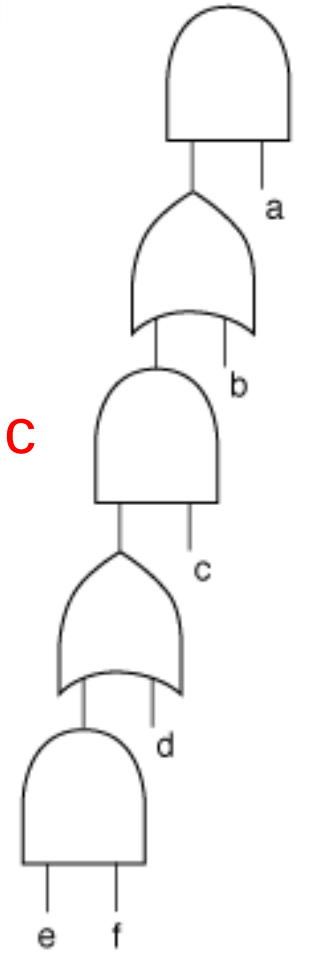
Logic gates are not simple nodes—some input changes don’t cause output changes.

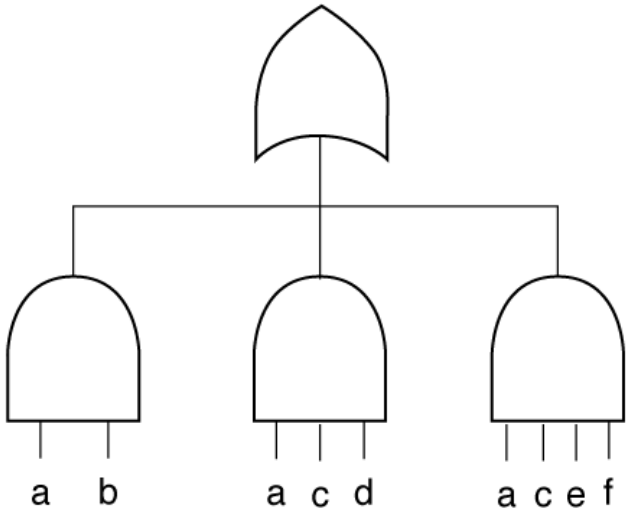
A false path is a path which cannot be exercised due to Boolean gate conditions.

False paths cause pessimistic delay estimates.

# Logic rewrites

deep logic




shallow logic

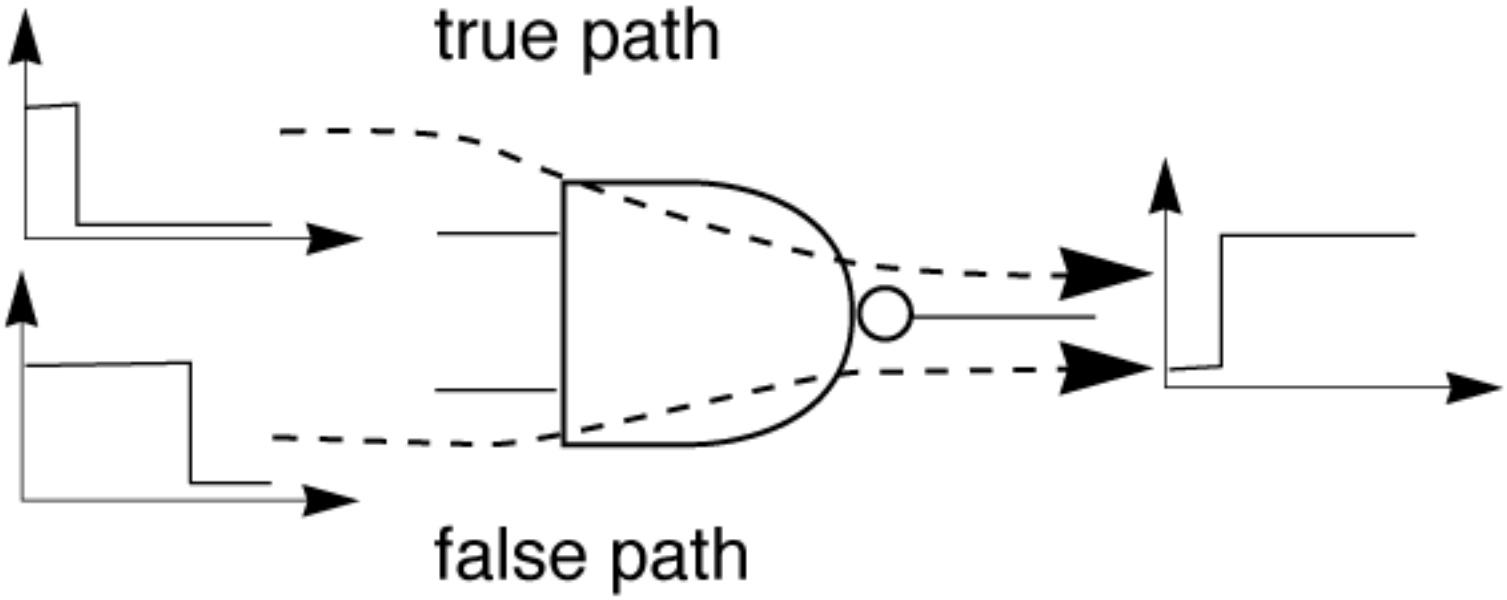
# Logic transformations

Can rewrite by using sub expressions.

Flattening logic increases gate fan-in.

Logic rewrites may affect gate placement.

# False path example



# Logic optimization

Logic synthesis programs transform Boolean expressions into logic gate networks in a particular library.

Optimization goals: minimize area, meet delay constraint.

# Technology-independent optimizations

Works on Boolean expression equivalence.

Estimates size based on number of literals.

Uses factorization, re-substitution, minimization, etc. to optimize logic.

Technology-independent phase uses simple delay models.

# Technology-dependent optimizations

Maps Boolean expressions into a particular cell library.

Mapping may take into account area, delay.

May perform some optimizations in addition to simple mapping.

Allows more accurate delay models.

# Tasks

Search design compilers for ASIC and FPGAs

- Student version
- Commercial