

# Tassadaq Hussain



# VLSI Design

## CMOS Transistor Theory



# Outline

Introduction

MOS Capacitor

nMOS I-V Characteristics

pMOS I-V Characteristics

Gate and Diffusion Capacitance

Pass Transistors

RC Delay Models



# Introduction

So far, we have treated transistors as ideal switches

An ON transistor passes a finite amount of current

Depends on terminal voltages

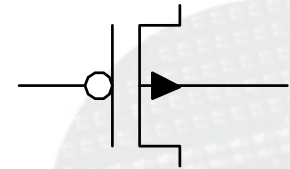
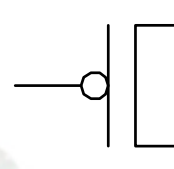
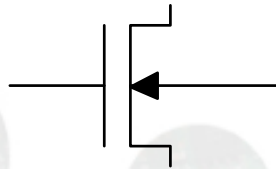
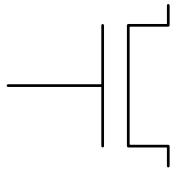
Derive current-voltage (I-V) relationships

Transistor gate, source, drain all have capacitance

$$I = C (\Delta V / \Delta t) \rightarrow \Delta t = (C / I) \Delta V$$

Capacitance and current determine speed

Also explore what a “degraded level” really means



# MOS Capacitor

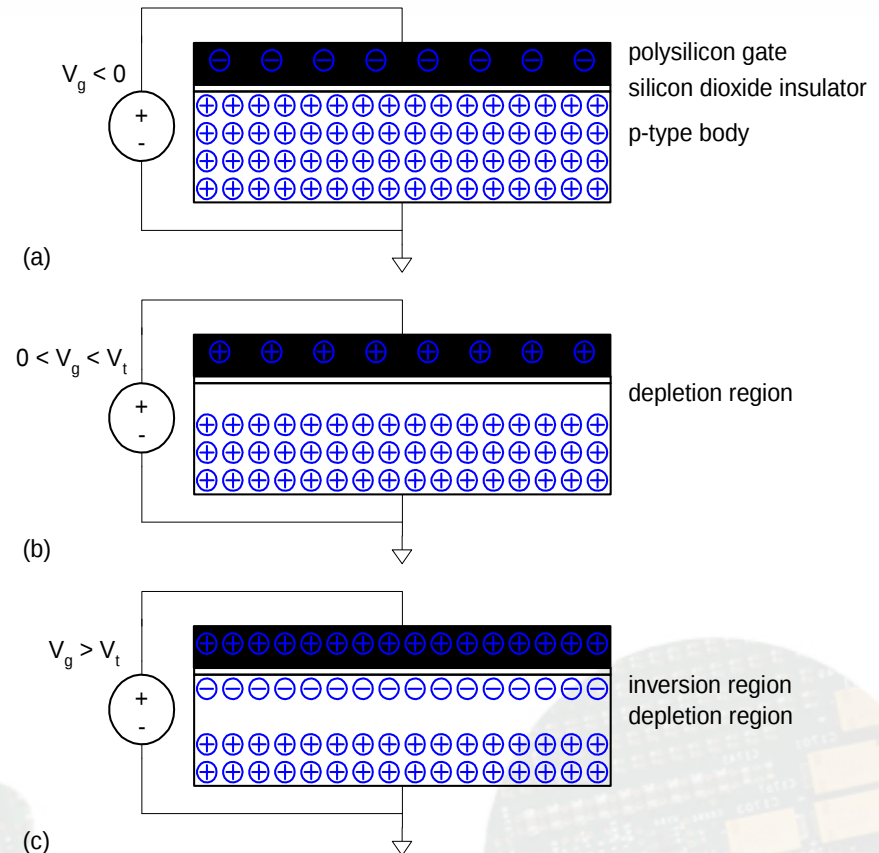
Gate and body form MOS capacitor

Operating modes

Accumulation

Depletion

Inversion



Example with an NMOS capacitor

Accumulation occurs typically for negative voltages where the negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface.

Depletion occurs for positive voltages; The positive charge on the gate pushes the mobile holes into the substrate, thereby depleting the semiconductor of the mobile carriers and leaving a negative charge in the space charge region which is due to the ionized acceptor ions.

The voltage separating the accumulation and depletion regime is referred to as the flatband voltage.

Inversion occurs at more positive voltages which are larger than the threshold voltage. In addition to the depletion layer charge a negatively charged inversion layer forms at the oxide-semiconductor interface.

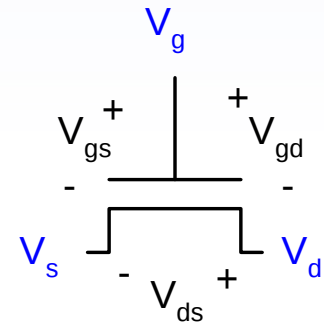
# Terminal Voltages

Mode of operation depends on  $V_g$ ,  $V_d$ ,  $V_s$

$$V_{gs} = V_g - V_s$$

$$V_{gd} = V_g - V_d$$

$$V_{ds} = V_d - V_s = V_{gs} - V_{gd}$$



Source and drain are symmetric diffusion terminals

However,  $V_{ds} \geq 0$

NMOS body is grounded. First assume source may be grounded or may be at a voltage above ground.

Three regions of operation

*Cutoff*

*Linear*

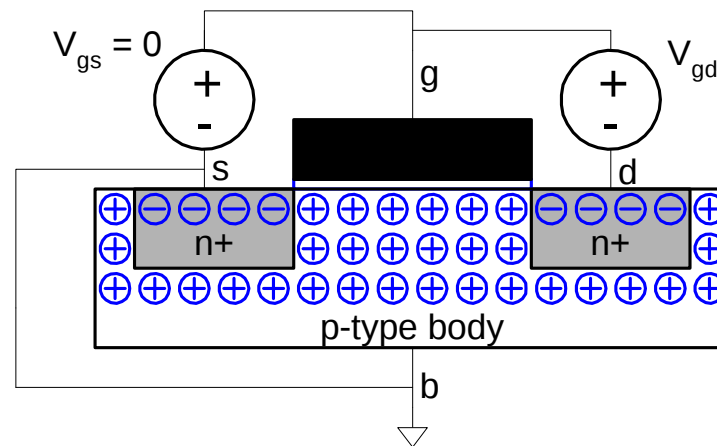
*Saturation*

# nMOS Cutoff

Let us assume  $v_s = v_d$

No channel, if  $v_{gs} = 0$

$$I_{ds} = 0$$





# NMOS Linear

Channel forms if  $V_{gs} > V_t$

No Current if  $V_{ds} = 0$

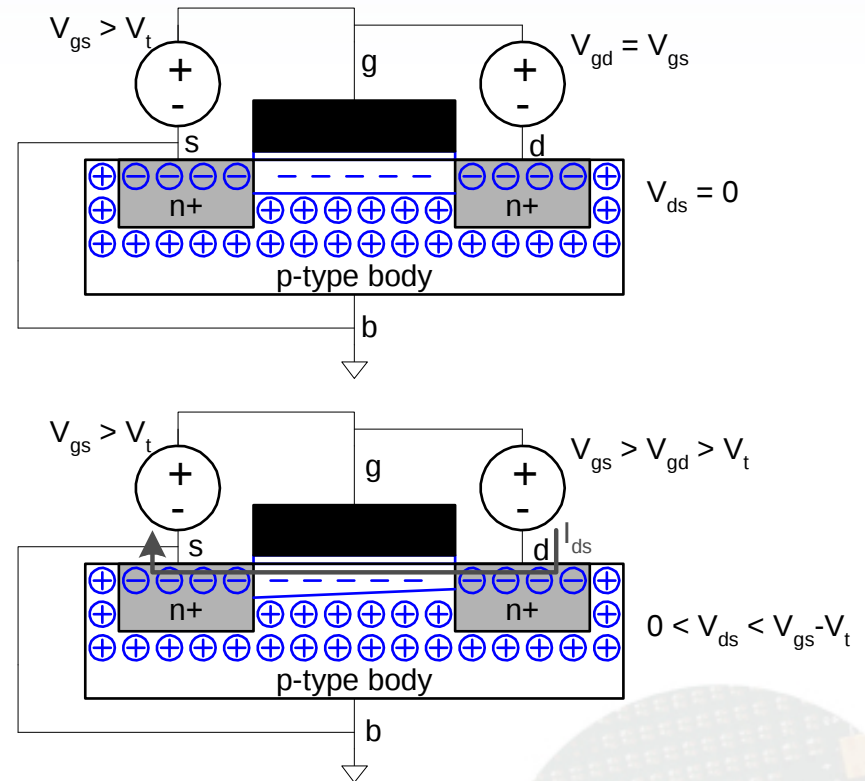
Linear Region:

If  $V_{ds} > 0$ , Current flows from d to s (e<sup>-</sup> from s to d)

$I_{ds}$  increases linearly

with  $V_{ds}$  if  $V_{ds} > V_{gs} - V_t$ .

Similar to linear resistor

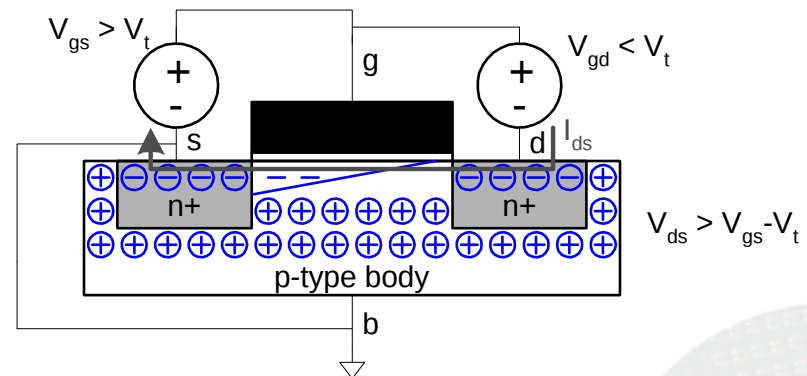


# NMOS Saturation

Channel pinches off if  $V_{ds} > V_{gs} - V_t$ .

$I_{ds}$  “independent” of  $V_{ds}$ , i.e., current saturates

Similar to current source



# I-V Characteristics

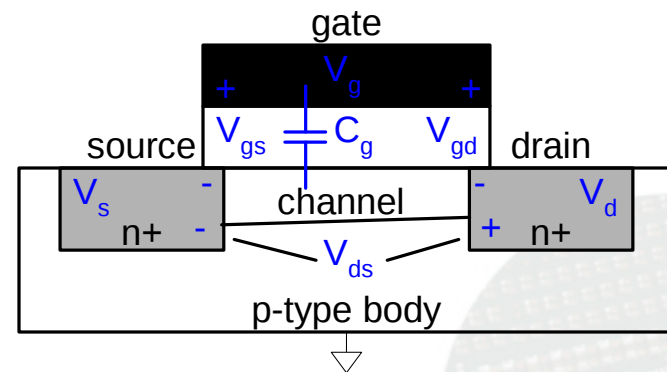
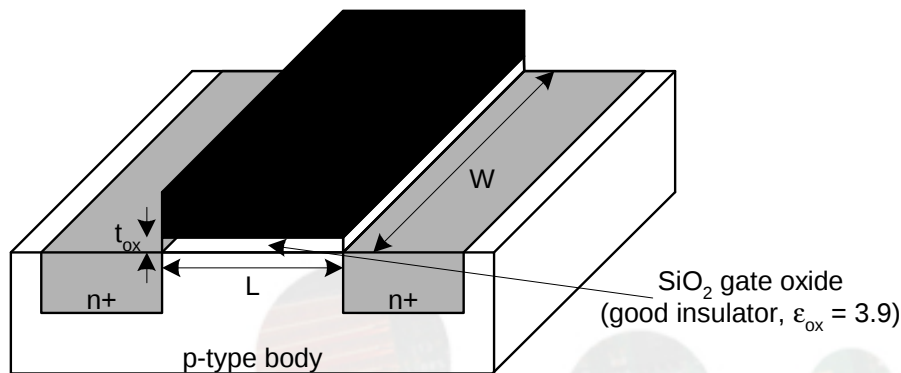
In Linear region,  $I_{ds}$  depends on  
How much charge is in the channel  
How fast is the charge moving

# Channel Charge

MOS structure looks like parallel plate capacitor while operating in inversion

Gate – oxide (dielectric) – channel

$$Q_{\text{channel}} =$$



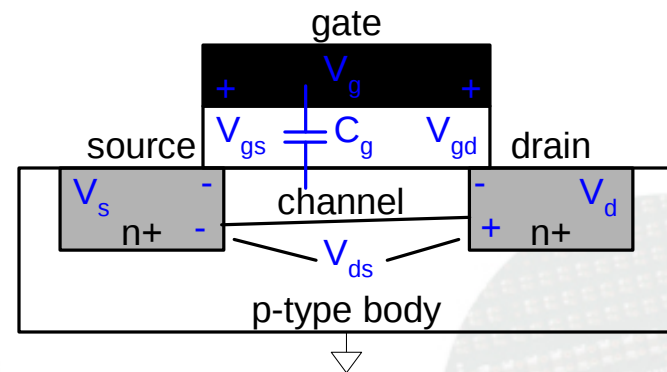
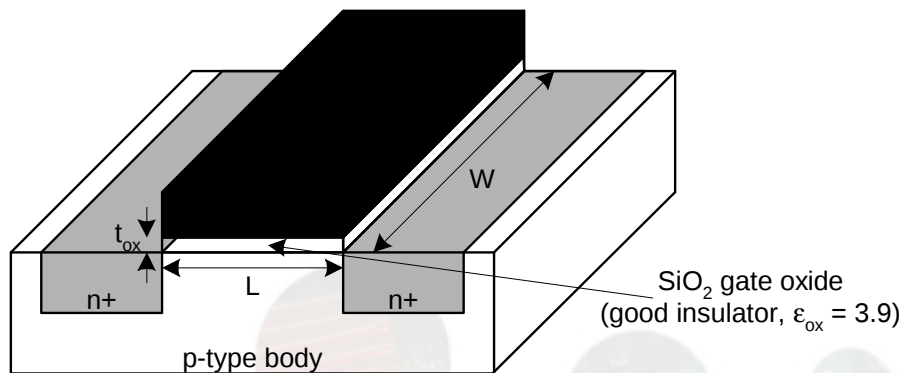
# Channel Charge

MOS structure looks like parallel plate capacitor while operating in inversion

Gate – oxide – channel

$$Q_{\text{channel}} = CV$$

$C =$



# Channel Charge

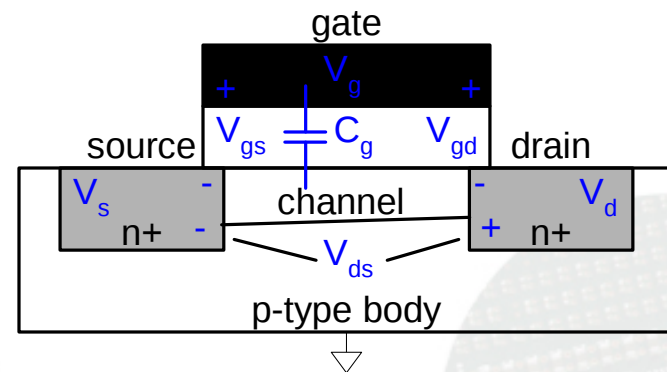
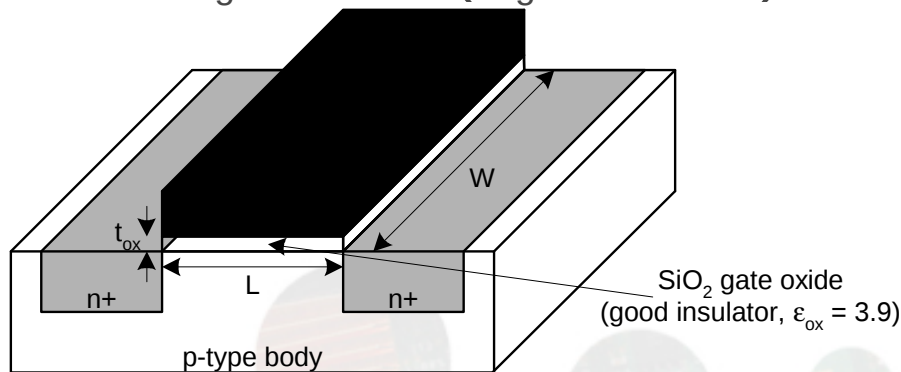
MOS structure looks like parallel plate capacitor while operating in inversion

Gate – oxide – channel

$$Q_{\text{channel}} = CV$$

$$C = C_g = \epsilon_{\text{ox}} WL/t_{\text{ox}} = C_{\text{ox}} WL$$

$$V = V_{\text{gc}} - V_t = (V_{\text{gs}} - V_{\text{ds}}/2) - V_t$$



# Carrier velocity

Charge is carried by e-

Carrier velocity  $v$  proportional to lateral E-field between source and drain

$$v = \mu E \quad \mu \text{ called mobility}$$

$$E = V_{ds}/L$$

Time for carrier to cross channel:

$$t = L / v$$

# NMOS Linear I-V

Now we know

How much charge  $Q_{\text{channel}}$  is in the channel

How much time  $t$  each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{\text{ox}} \frac{W}{L} \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$$= \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$



# NMOS Saturation I-V

If  $V_{gd} < V_t$ , channel pinches off near drain

When  $V_{ds} > V_{dsat} = V_{gs} - V_t$

Now drain voltage no longer increases current

$$\begin{aligned} I_{ds} &= \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat} \\ &= \frac{\beta}{2} (V_{gs} - V_t)^2 \end{aligned}$$

# NMOS I-V Summary

*Shockley* 1<sup>st</sup> order transistor models (valid for Large channel devices only)

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

# Example

For a 0.6  $\mu\text{m}$  process ([MOSIS site](#))

From AMI Semiconductor

$$t_{\text{ox}} = 100 \text{ \AA}$$

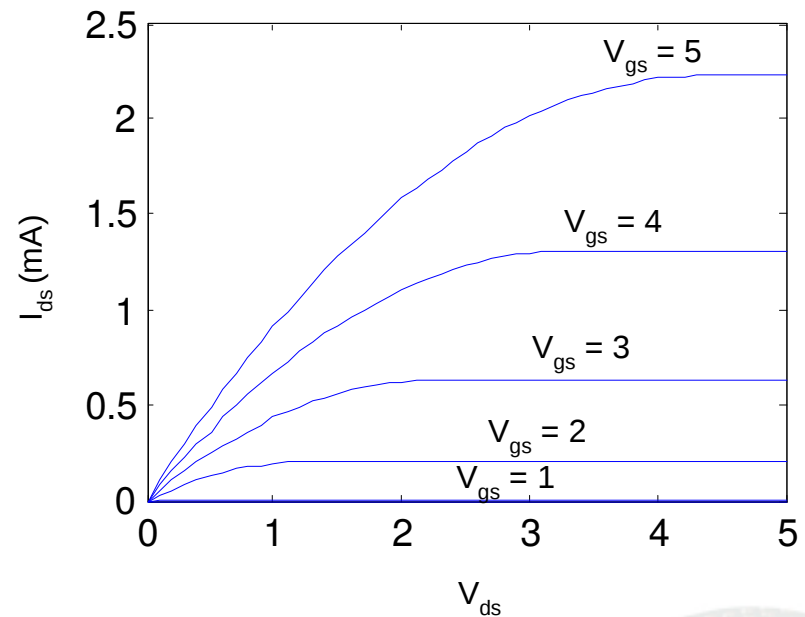
$$\mu = 350 \text{ cm}^2/\text{V}^*\text{s}$$

$$V_t = 0.7 \text{ V}$$

Plot  $I_{\text{ds}}$  vs.  $V_{\text{ds}}$

$$V_{\text{gs}} = 0, 1, 2, 3, 4, 5$$

$$\text{Use } W/L = 4/2 \lambda$$



$$\beta = \mu C_{\text{ox}} \frac{W}{L} = (350) \left( \frac{3.9 \cdot 8.85 \times 10^{-14}}{100 \times 10^{-8}} \right) \left( \frac{W}{L} \right) = 120 \frac{W}{L} \mu\text{A}/\text{V}^2$$

# PMOS I-V

All dopings and voltages are inverted for PMOS

Mobility  $\mu_p$  is determined by holes

Typically 2-3x lower than that of electrons  $\mu_n$

120 cm<sup>2</sup>/V\*s in AMI 0.6  $\mu$ m process

Thus PMOS must be wider to provide same current

In this class, assume  $\mu_n / \mu_p = 2$

# Capacitance

Any two conductors separated by an insulator have capacitance

Gate to channel capacitor is very important

Creates channel charge necessary for operation

Source and drain have capacitance to body

Across reverse-biased diodes

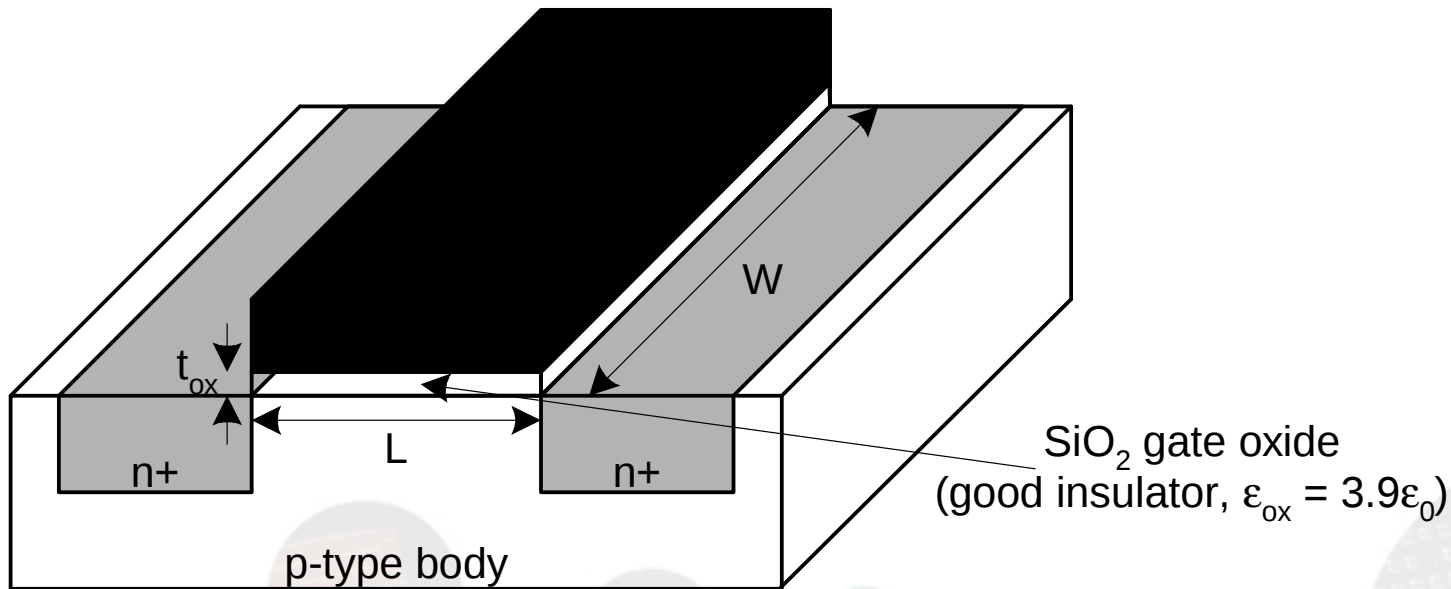
Called diffusion capacitance because it is associated with source/drain diffusion

# Gate Capacitance

Approximate channel as connected to source

$$C_{gs} = \epsilon_{ox} WL/t_{ox} = C_{ox} WL = C_{permicron} W$$

$C_{permicron}$  is typically about 2 fF/ $\mu\text{m}$



# Diffusion Capacitance

$C_{sb}$ ,  $C_{db}$

Undesirable, called *parasitic* capacitance

Capacitance depends on area and perimeter

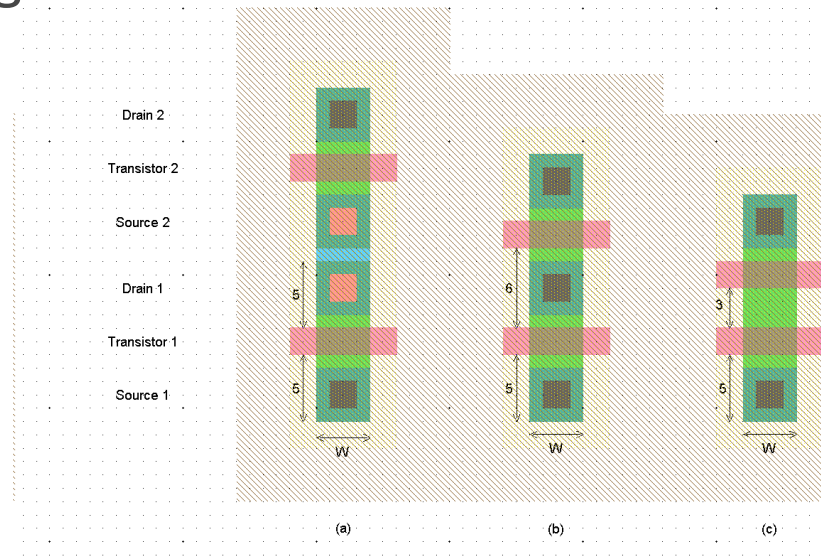
Use small diffusion nodes

Comparable to  $C_g$

for contacted diff

$\frac{1}{2} C_g$  for uncontacted

Varies with process

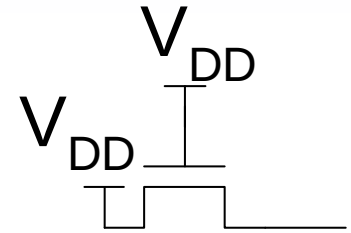


# Pass Transistors

We have assumed source is grounded

What if source  $> 0$ ?

e.g. pass transistor passing  $V_{DD}$





# NMOS Pass Transistors

We have assumed source is grounded

What if source  $> 0$ ?

e.g. pass transistor passing  $V_{DD}$

Let  $V_g = V_{DD}$

Now if  $V_s > V_{DD} - V_t$ ,  $V_{gs} < V_t$

Hence transistor would turn itself off

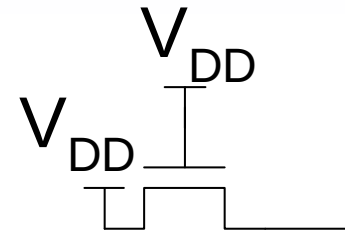
NMOS pass transistors **pull-up** no higher than  $V_{DD} - V_{tn}$

Called a degraded “1”

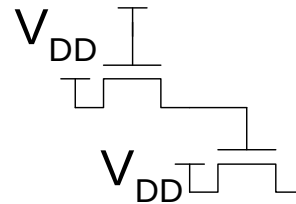
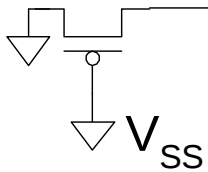
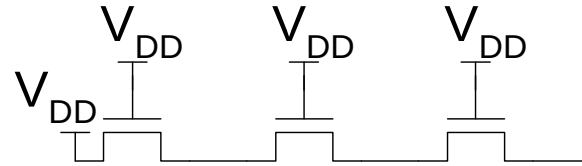
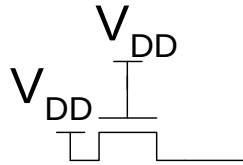
Approach degraded value slowly (low  $I_{ds}$ )

PMOS pass transistors **pull-down** no lower than  $V_{tp}$

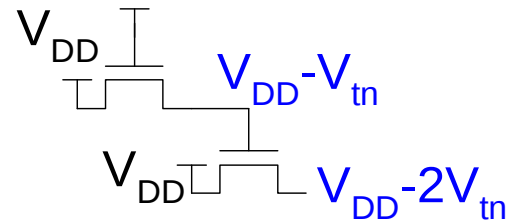
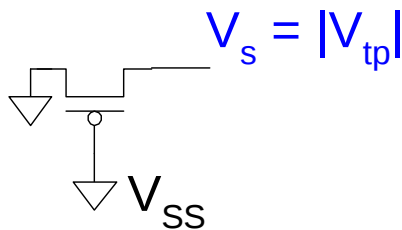
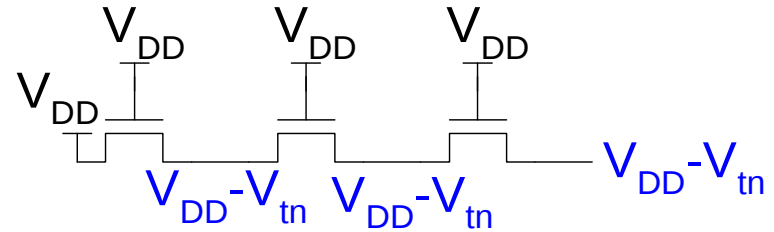
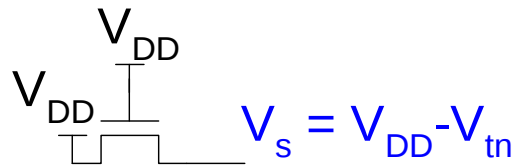
Called a degraded “0”



# Pass Transistor Ckts



# Pass Transistor Ckts



# Effective Resistance

Shockley models have limited value

Not accurate enough for modern transistors

Too complicated for much hand analysis

Simplification: treat transistor as resistor

Replace  $I_{ds}(V_{ds}, V_{gs})$  with effective resistance  $R$

- $I_{ds} = V_{ds}/R$

$R$  averaged across switching of digital gate

Too inaccurate to predict current at any given time

But good enough to predict RC delay

# RC Delay Model

Use equivalent circuits for MOS transistors

Ideal switch + capacitance and ON resistance

Unit nMOS has resistance  $R$ , capacitance  $C$

Unit pMOS has resistance  $2R$ , capacitance  $C$

Capacitance proportional to width

Resistance inversely proportional to width



# RC Values

Capacitance

$C = C_g = C_s = C_d = 2 \text{ fF}/\mu\text{m}$  of gate width

Values similar across many processes

Resistance

$R \approx 6 \text{ K}\Omega \cdot \mu\text{m}$  in 0.6 $\mu\text{m}$  process

Improves with shorter channel lengths

Unit transistors

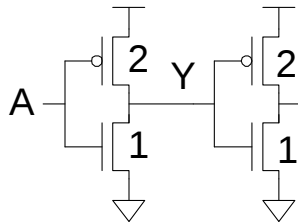
May refer to minimum contacted device ( $4/2 \lambda$ )

Or maybe 1  $\mu\text{m}$  wide device

Doesn't matter as long as you are consistent

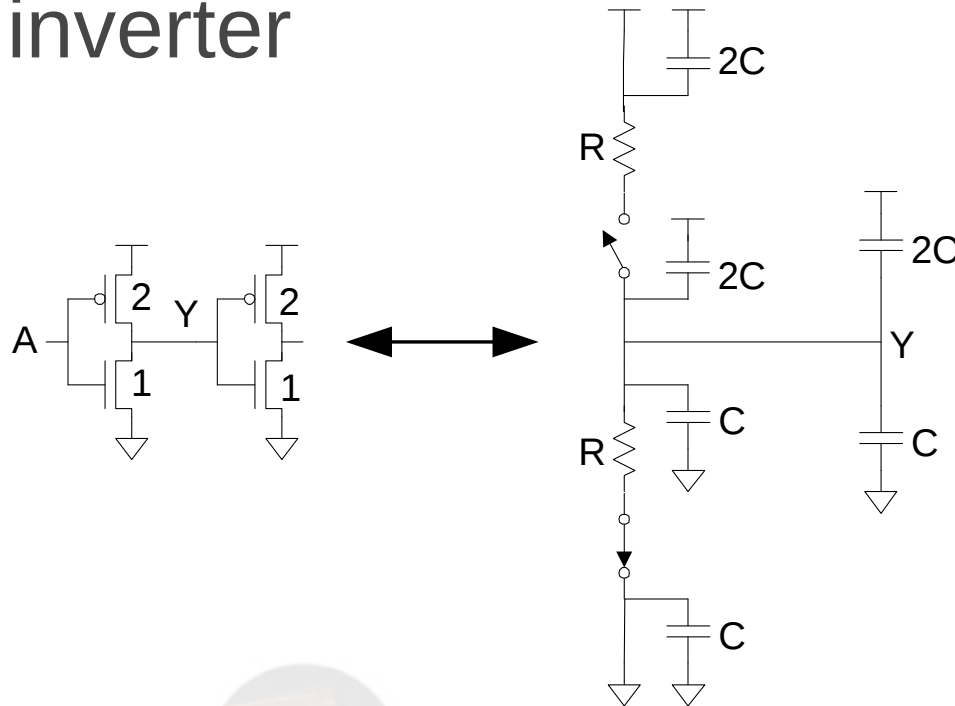
# Inverter Delay Estimate

Estimate the delay of a fanout-of-1 inverter



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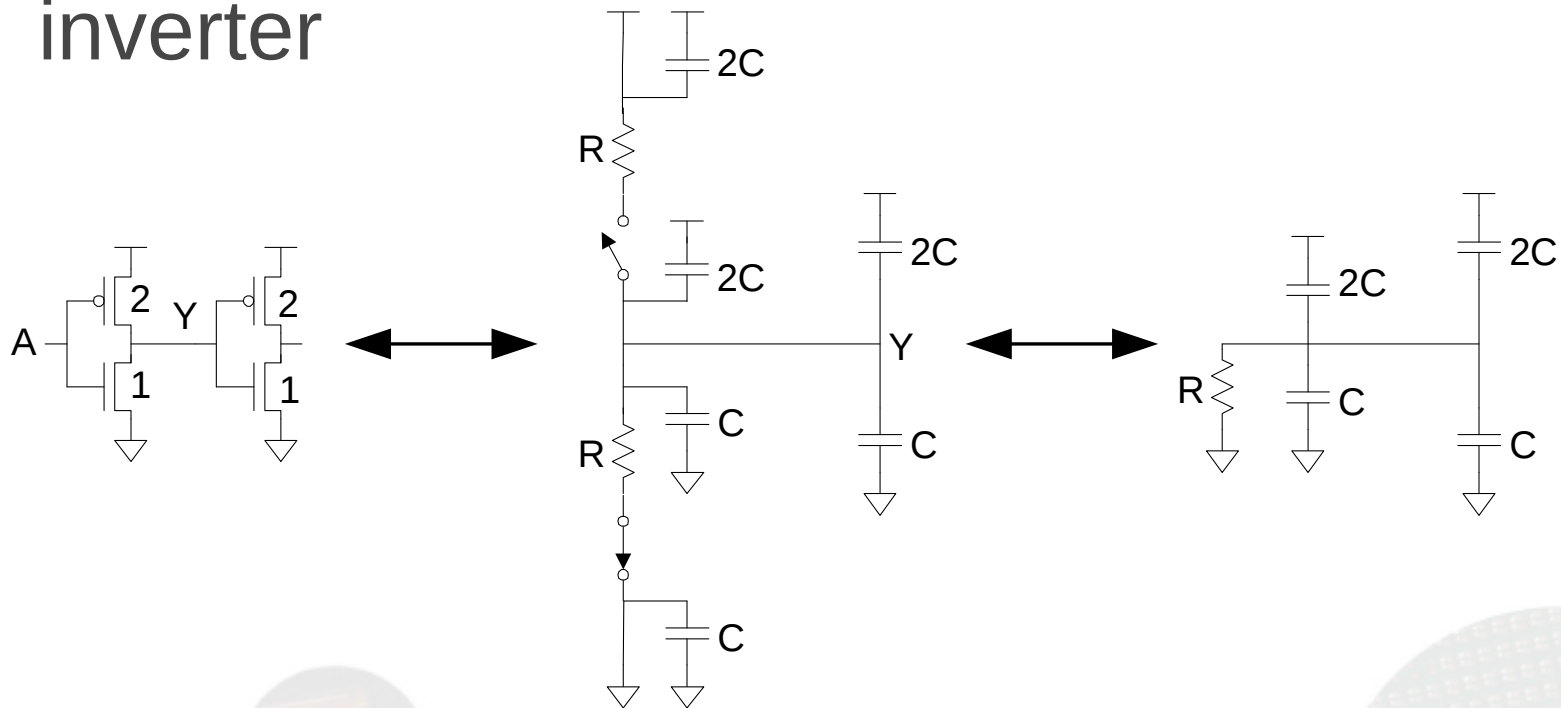
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