Introduction to Data Acquisition System

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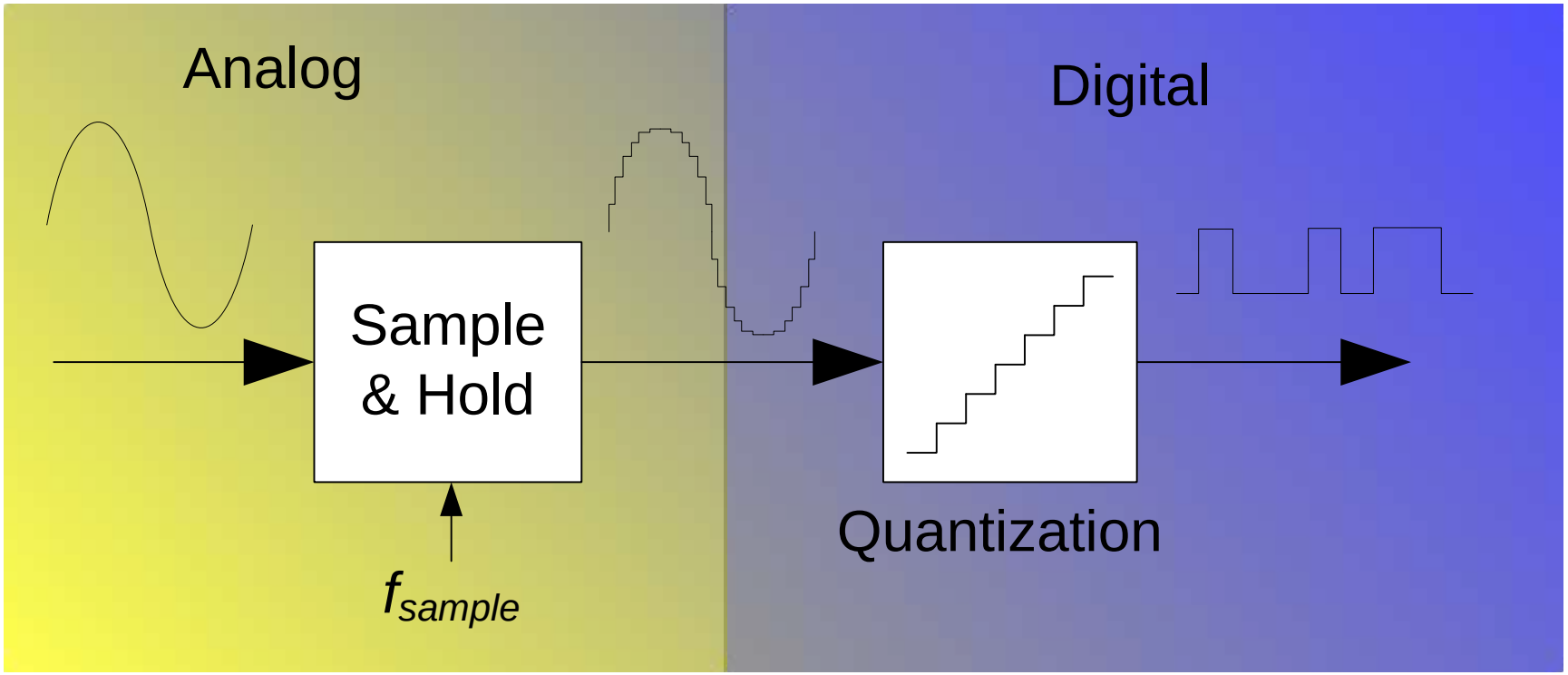
Agenda

- Introduction
- DAS Blocks
- Characteristic Values of ADCs
- Nyquist-Rate ADCs
- Oversampling ADC
- Practical Issues
- Low Power ADC Design

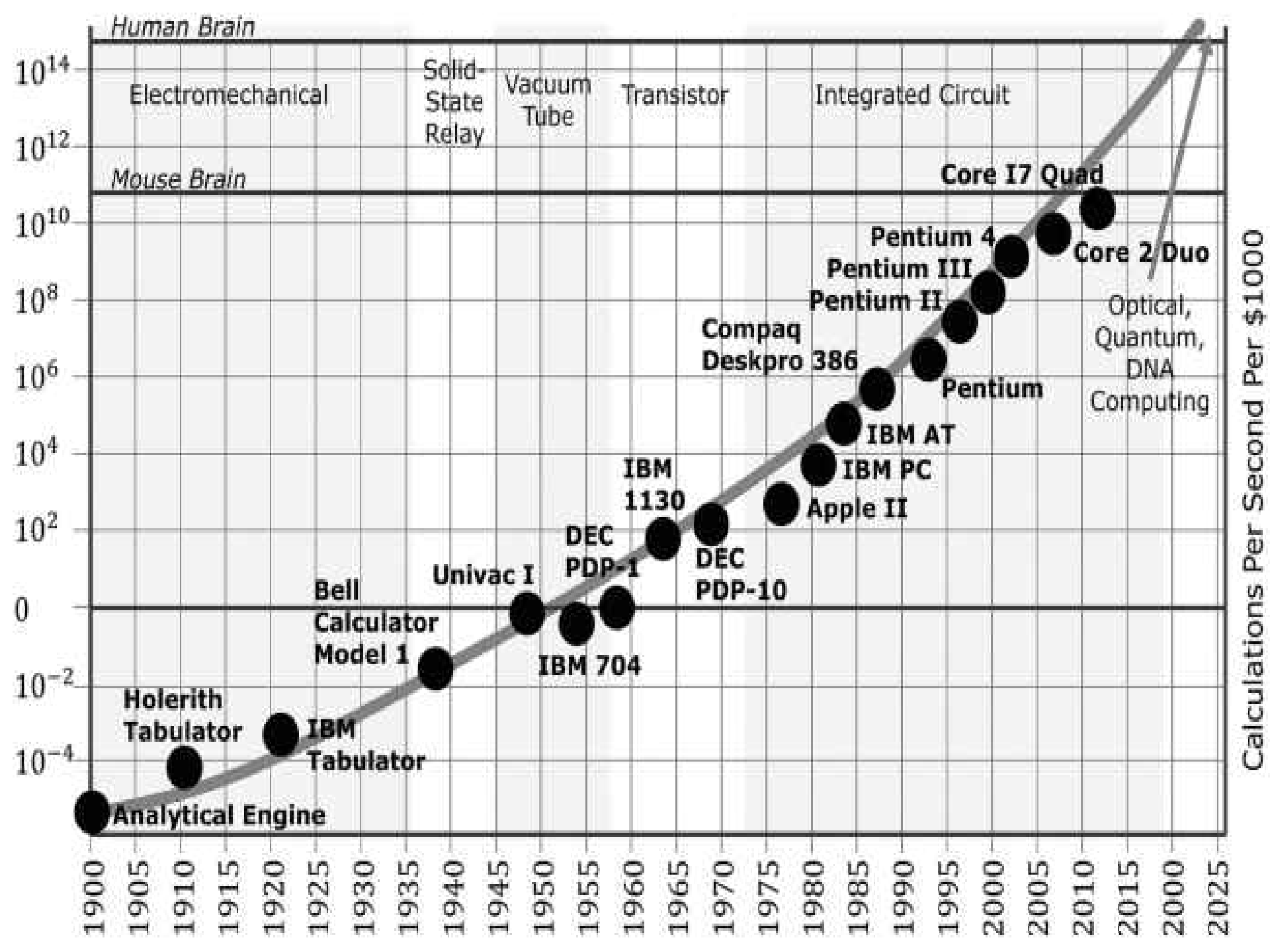
Introduction

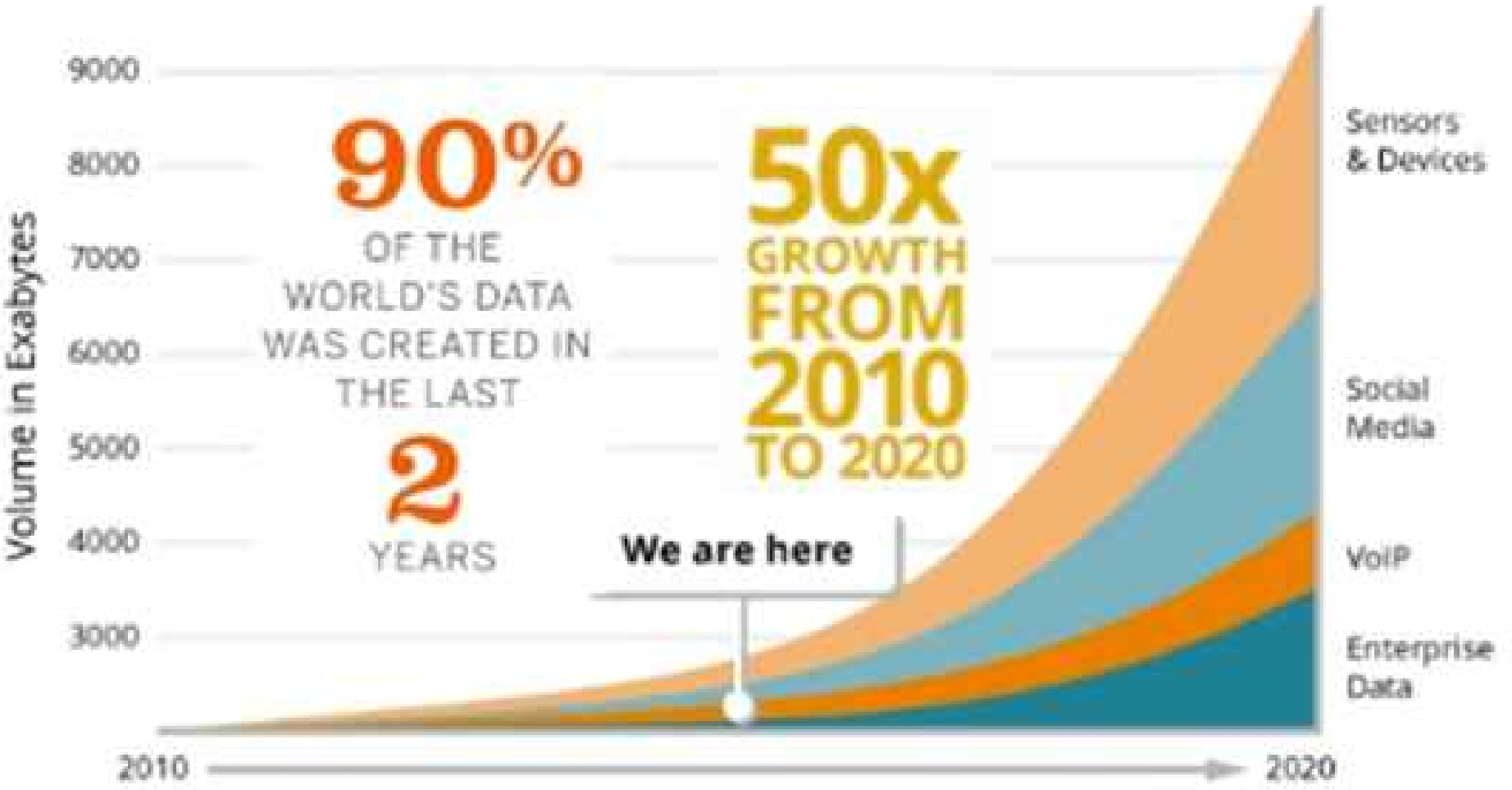
- ADC = **A**nalog-**D**igital-**C**onverter
- Conversion of audio signals (mobile micro, digital music records, ...)
- Conversion of video signals (cameras, frame grabber, ...)
- Measured value acquisition (temperature, pressure, luminance, ...)

ADC - Scheme



- Analog input can be voltage or current (*in the following only voltage*)
- Analog input can be positive or negative (*in the following only positive*)


Human Brain
Mouse Brain
Electromechanical
Solid-State Relay
Vacuum Tube
Transistor
Integrated Circuit
Optical, Quantum, DNA Computing
Core I7 Quad
Core 2 Duo
Pentium 4
Pentium III
Pentium II
Pentium
Compaq Deskpro 386
IBM AT
IBM PC
Apple II
IBM 1130
DEC PDP-1
DEC PDP-10
Univac I
IBM 704
Bell Calculator Model 1
Holerith Tabulator
IBM Tabulator
Analytical Engine
10^{14}
10^{12}
10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
0
10^{-2}
10^{-4}
1900 1905 1910 1915 1920 1925 1930 1935 1940 1945 1950 1955 1960 1965 1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2000 2025
Calculations Per Second Per $1000


Volume in Exabytes
9000
8000
7000
6000
5000
4000
3000
90%
OF THE WORLD'S DATA WAS CREATED IN THE LAST
2
YEARS
50x
GROWTH FROM 2010 TO 2020
We are here
Sensors & Devices
Social Media
VoIP
Enterprise Data
2010
2020

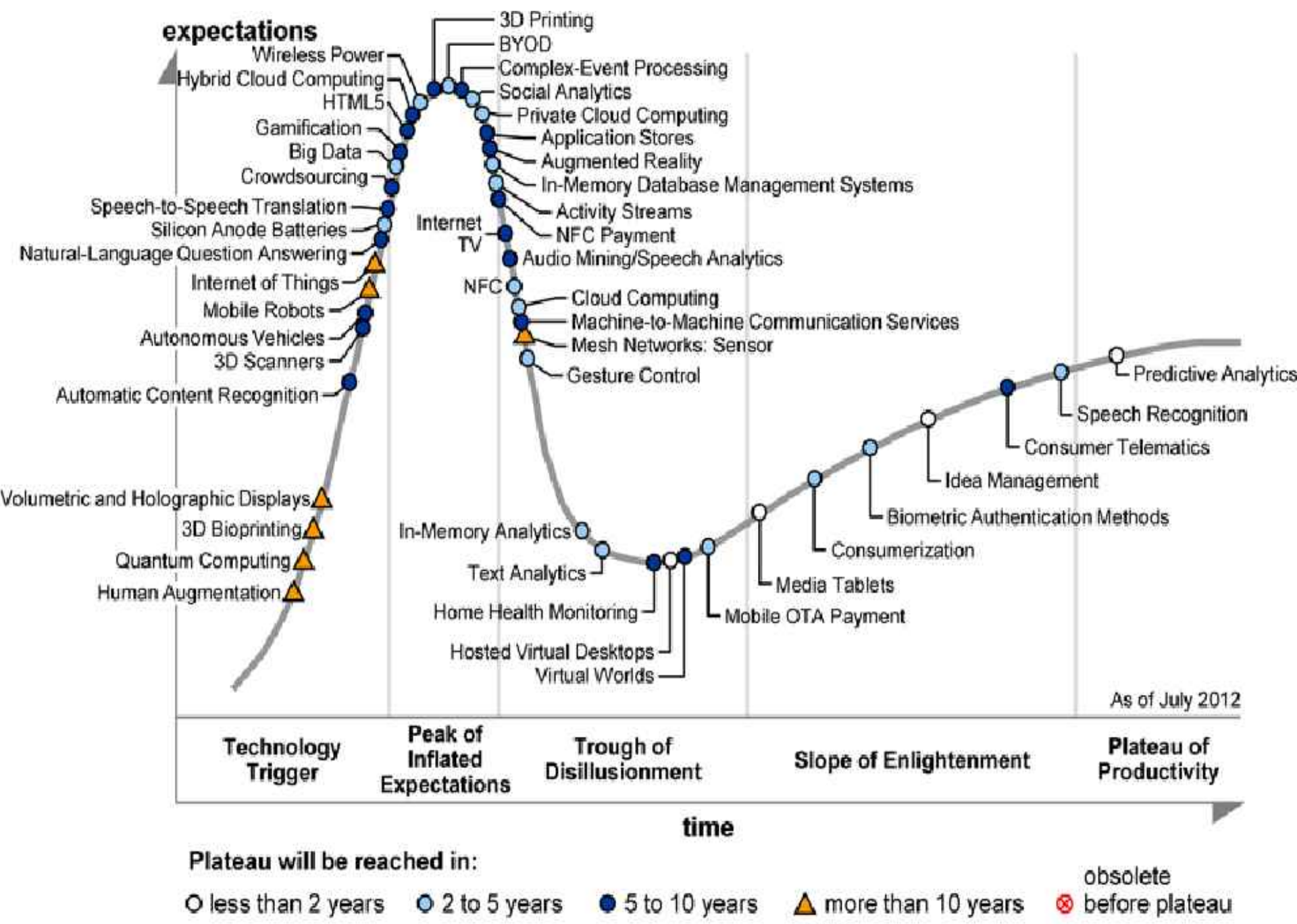
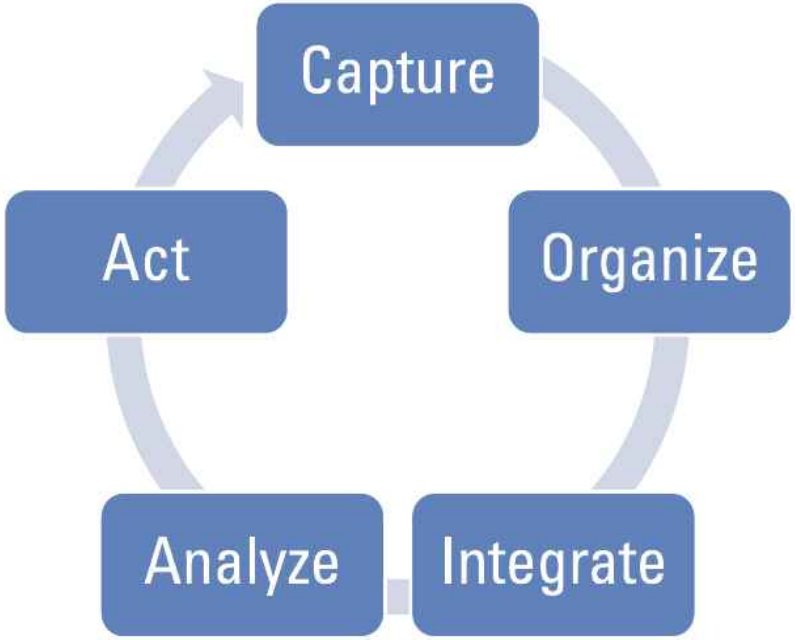
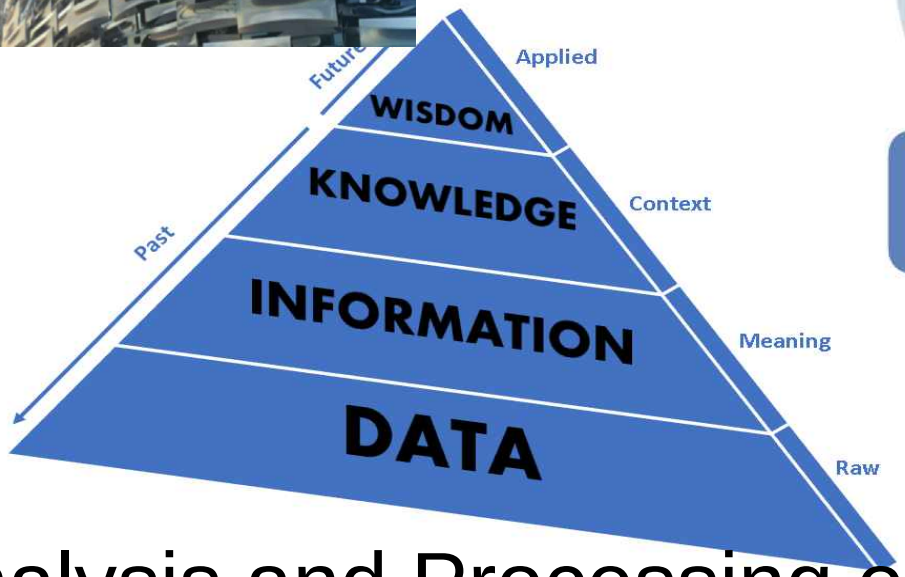


Figure 1: Gartner Hype cycle [11]

Big Data





Analysis and Processing of Big Data are changing the energy market map

DAS

Figure 3 Interfaced with variety of SBC

Stages of DAS

- Signal Conditioning
  - To improve the quality of signals in terms of amplification, linearization, compensation, filtering, and attenuation.
- Buffering
- Amplification
- Multiplexing
- ADC

2. Characteristic Values of ADCs

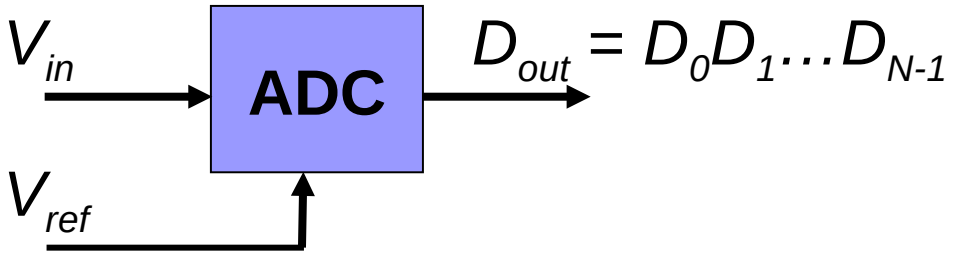
- Which values characterize an ADC?
- What kind of errors exist?
- What is aliasing?

ADC Values

- **Resolution N:** number of discrete values to represent the analog values (in Bit)
  - 8 Bit = 2^8 = 256 quantization level,
  - 10 Bit = 2^{10} = 1024 quantization level
- **Reference voltage V_{ref}:** Analog input signal V_{in} is related to digital output signal D_{out} through V_{ref} with:

$$V_{in} = V_{ref} \cdot (D_0 2^{-1} + D_1 2^{-2} + \ldots + D_{N-1} 2^{-N})$$

  - Example: N = 3 Bit, V_{ref} = 1V, D_{out} = '011'
    => V_{in} = 1V · (2^{-2} + 2^{-3}) = 1V · (0.25 + 0.125) = 0.375V



ADC Values cont'd

- V_{LSB} : Minimum measurable voltage difference in ideal case (LSB – least significant Bit)
  - $V_{LSB} = V_{ref} / 2^N$
  - $V_{in} = V_{LSB} (D_0 2^{N-1} + D_1 2^{N-2} + \ldots + D_{N-1} 2^0)$
  - Example: N = 3 Bit, V_{ref} = 1V, D_{out} = '011'

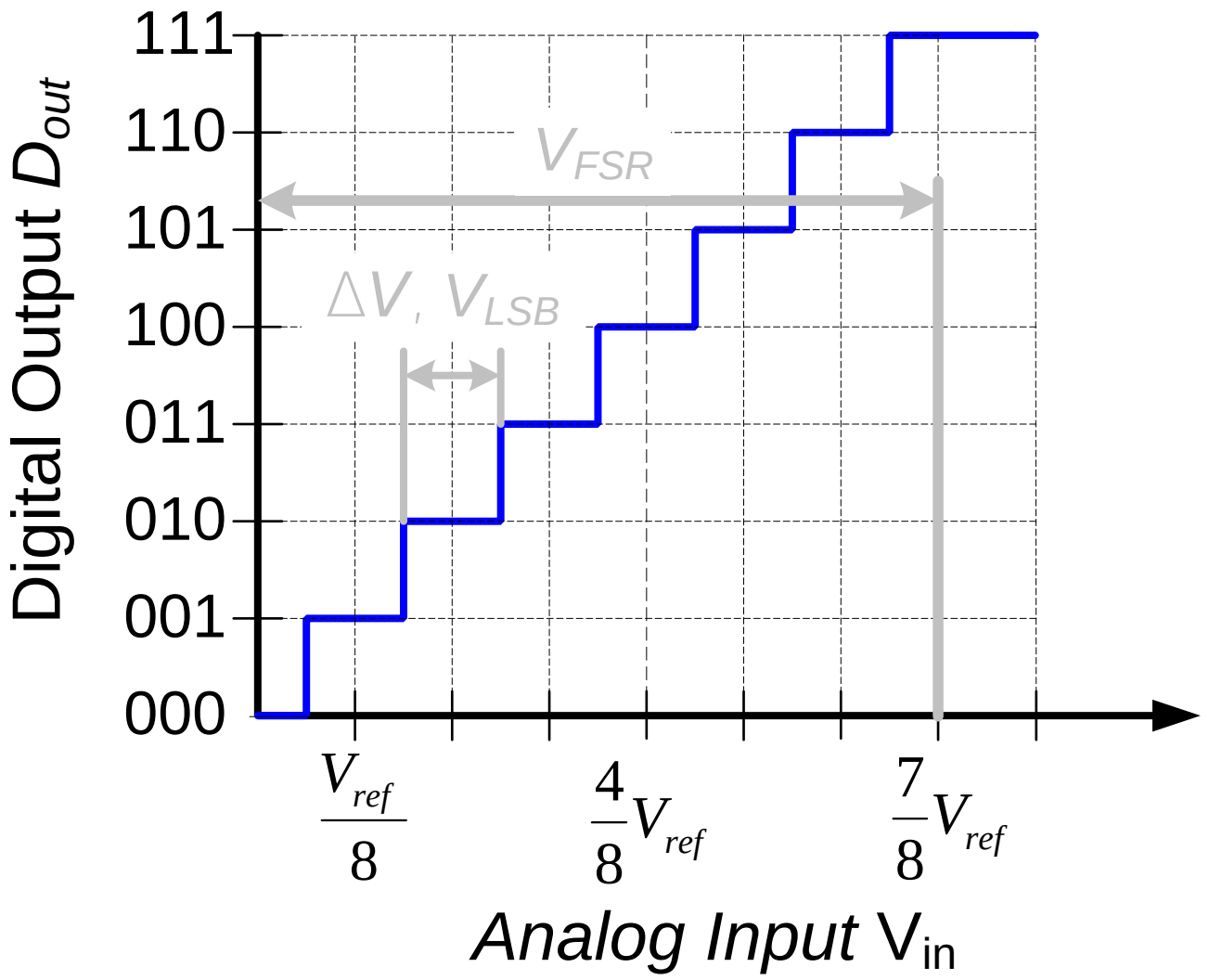
    => $V_{LSB} = 1V / 2^3 = 0.125V$

    => $V_{in} = 0.125V \cdot (2^1 + 2^0) = 0.125V \cdot 3 = 0.375V$
- **ΔV:** Voltage difference between two logic level
  - Ideal: all $\Delta V = V_{LSB}$
- V_{FSR} : Difference between highest and lowest measurable voltages (FSR – full scale range)

ADC Values cont'd

- ***SNR:*** Signal to Noise Ratio
  - Ratio of signal power to noise power
  - $SNR = \frac{P_{signal}}{P_{noise}}$, $SNR|_{db} = 10\log\left(\frac{P_{signal}}{P_{noise}}\right)$
- ***ENOB*****:** Effective Number of Bits
  - Effective resolution of ADC under observance of all noise and distortions
  - SINAD (SIgnal to Noise And Distortion) → ratio of fundamental signal to the sum of all distortion and noise (DC term removed)
  - Comparison of SINAD of ideal and real ADC with same word length

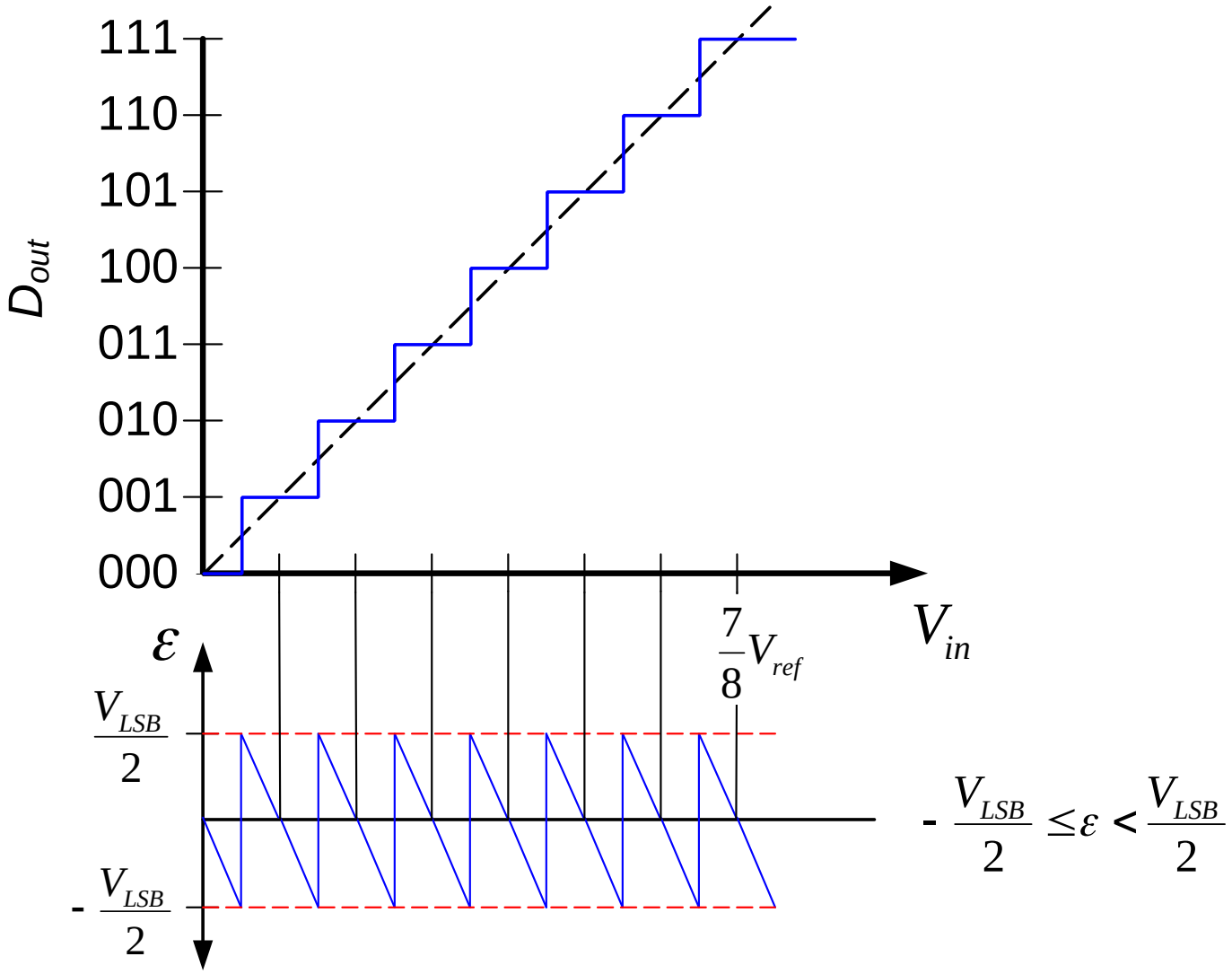
Ideal ADC


Digital Output D_{out}
111
110
101
100
011
010
001
000
V_{FSR}
ΔV, V_{LSB}
$\frac{V_{ref}}{8}$
$\frac{4}{8}V_{ref}$
$\frac{7}{8}V_{ref}$
Analog Input V_{in}

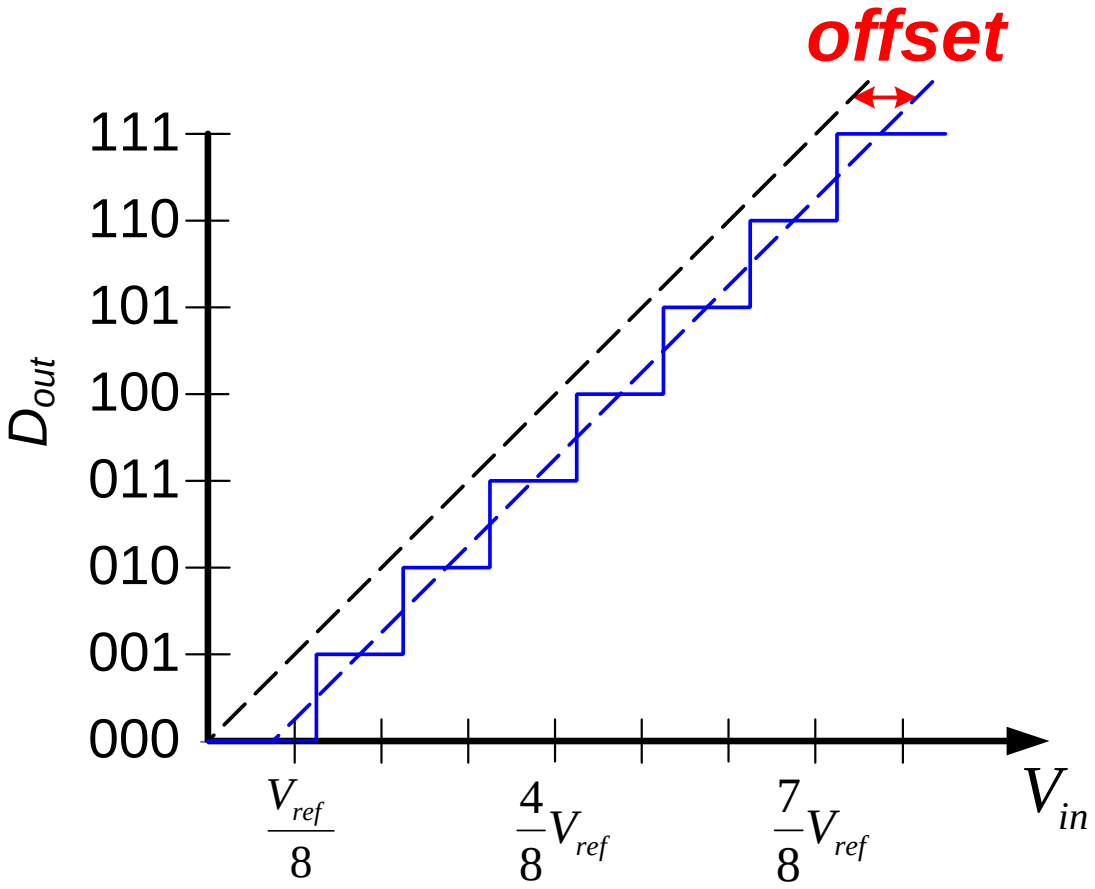
Further ADC Values

- **Bandwidth:** Maximum measurable frequency of the input signal
- **Power dissipation**
- **Conversion Time**: Time for conversion of an analog value into a digital value (*interesting in pipeline and parallel structures*)
- **Sampling rate (f_{samp}): R**ate at which new digital values are sampled from the analog signal (also: sample
- **Errors:** Quantization, offset, gain, INL, DNL, missing codes, non-monotonicity…

Quantization Error ε

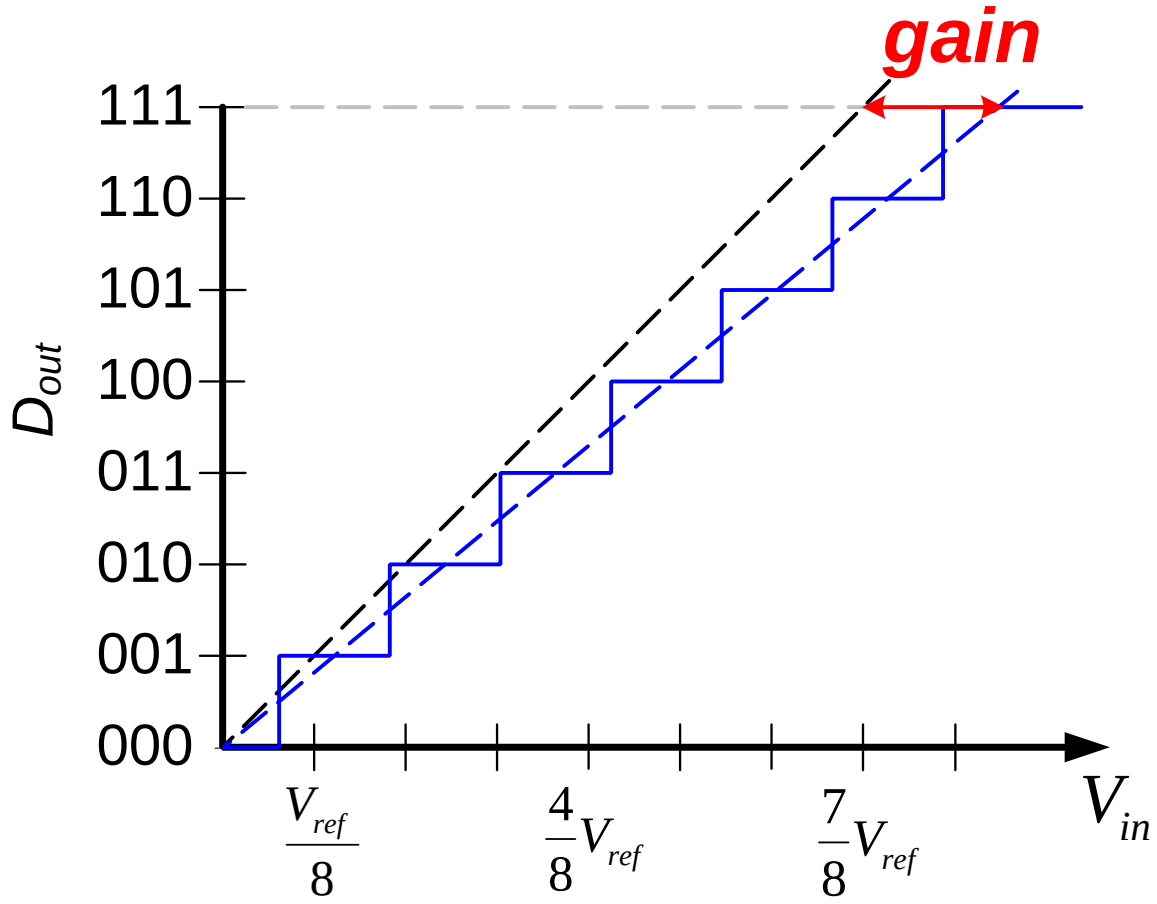


Offset Error



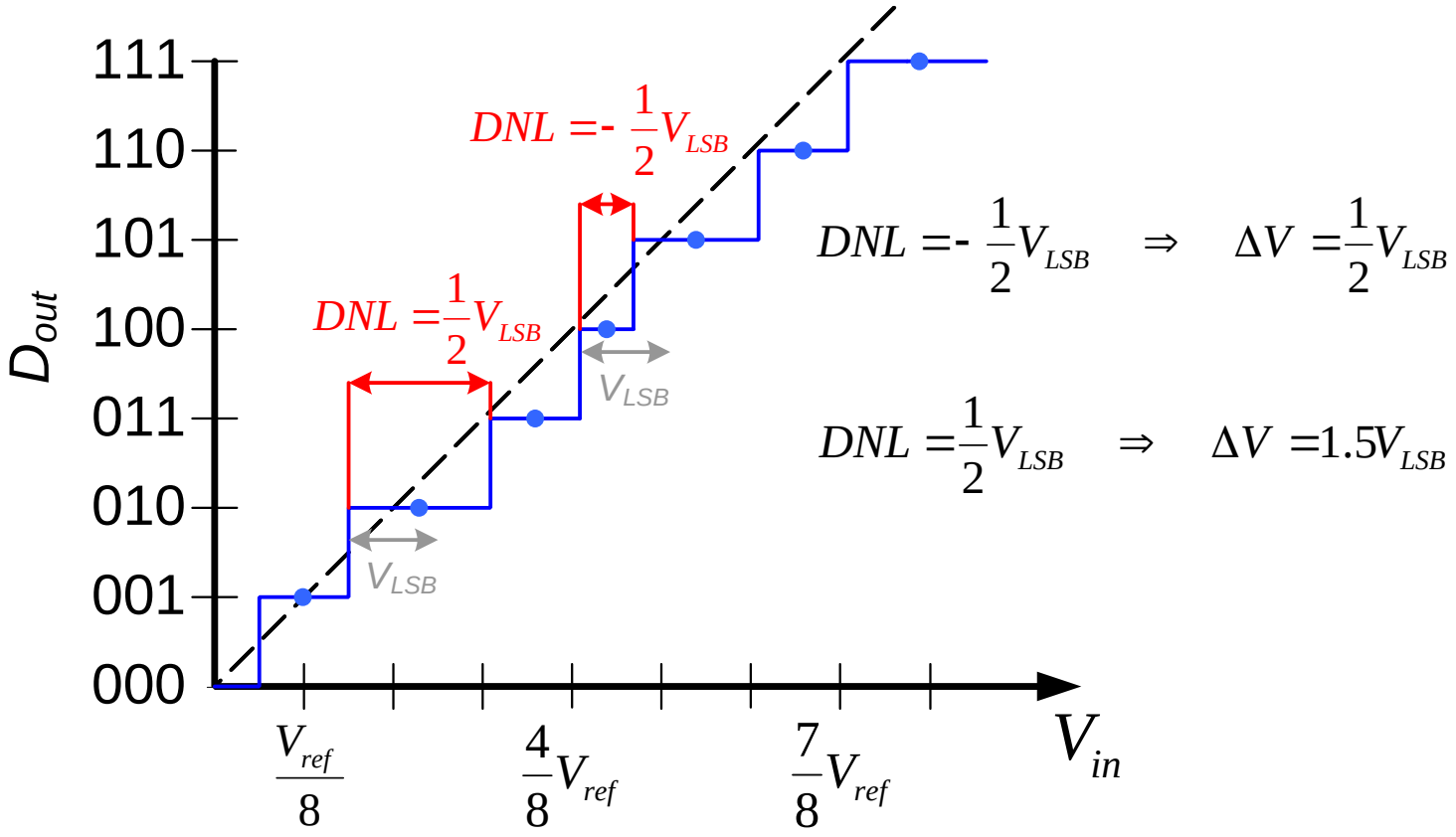
- Parallel shift of the whole curve
- E.g. caused by difference in ground line voltages

Gain Error



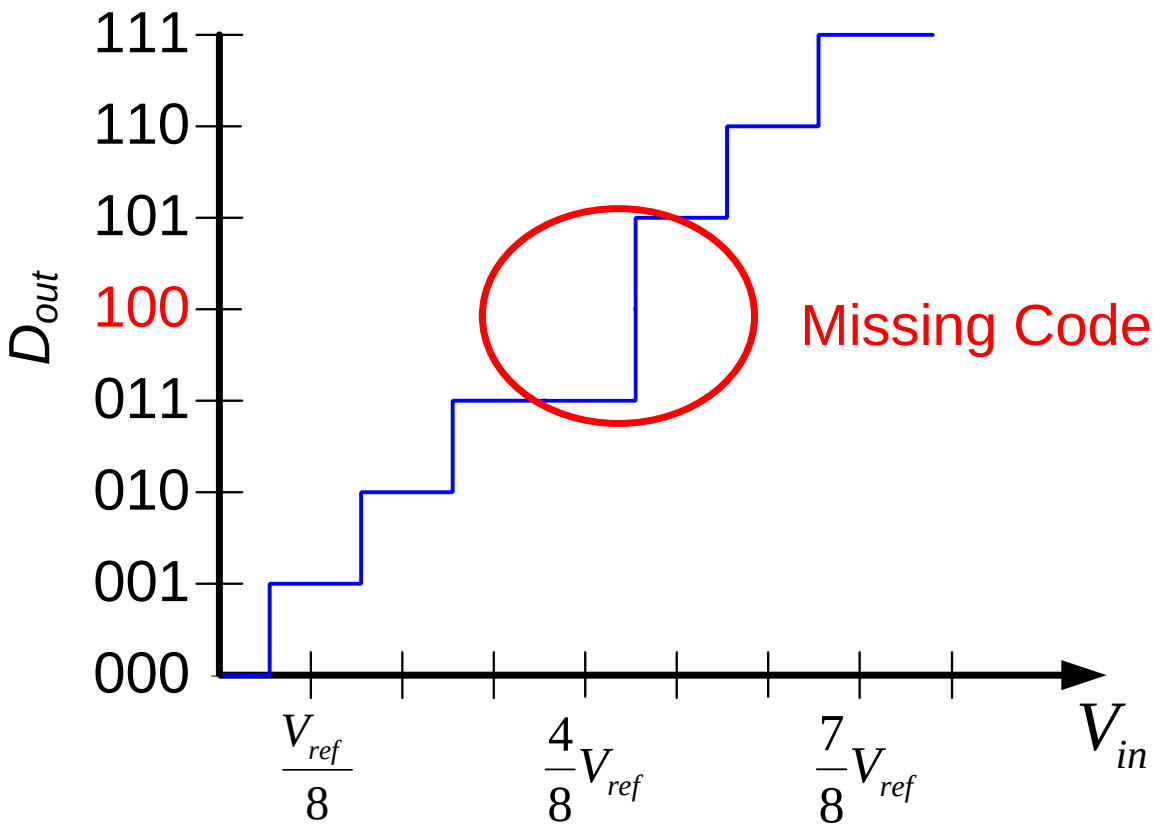
- Corresponds to too small or to large but equal ΔV
- E.g. caused by too small or too large V_{ref}

Differential Non-Linearity (DNL)



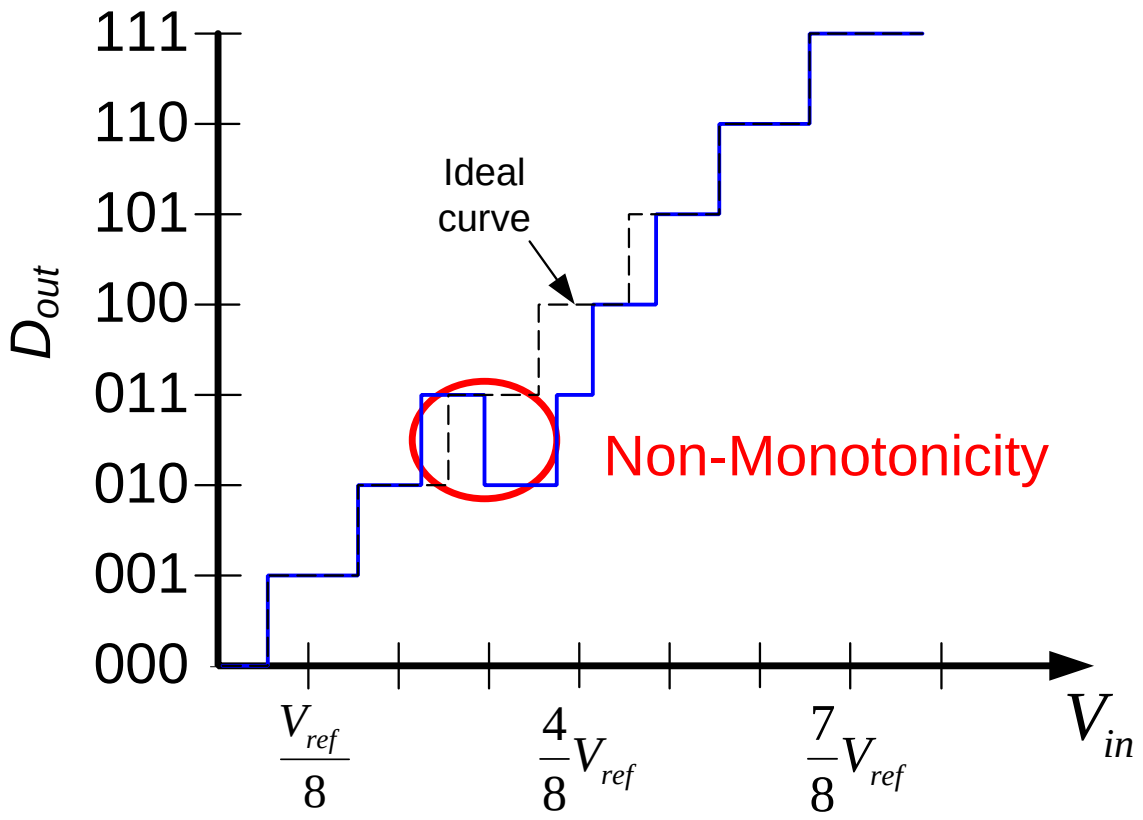
- Deviation of ΔV from V_{LSB} value (**in V_{LSB}**)
- Defined after removing of gain
- E.g. Caused by mismatch of the reference elements

Missing Codes



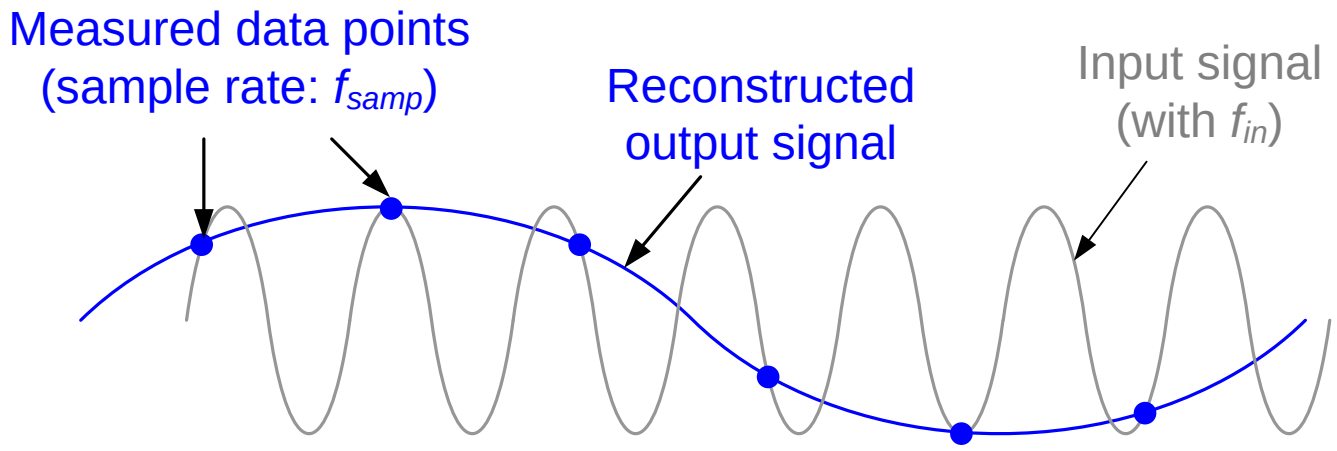
- Some bit combinations never appear
- Occurs, if maximum DNL > 1 V_{LSB} or maximum INL > 0.5 V_{LSB}

Non-Monotonicity



- Lower conversion result for a higher input voltage
- Includes that same conversion may result from two separate voltage ranges

Aliasing



- Too small sampling rate f_{samp} (under-sampling) can lead to aliasing (= frequency of reconstructed signal is to low)
- Nyquist criterion:
  - f_{samp} more than two times higher than highest frequency component f_{in} of input signal: $f_{samp} > 2 \cdot f_{in}$

3. Nyquist-Rate ADCs

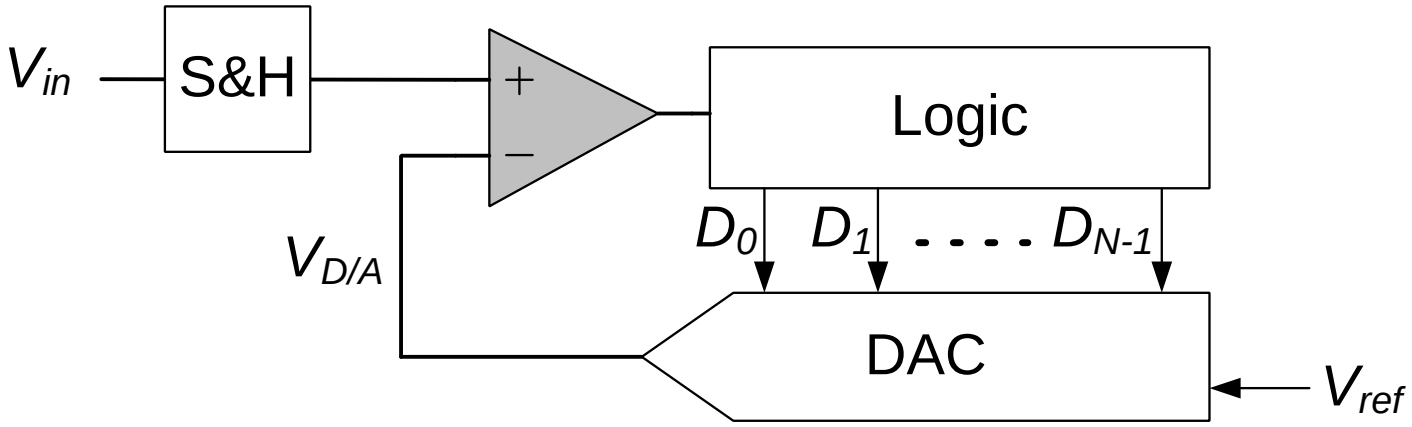
- How can Nyquist-rate ADCs be grouped?
- What is a dual slope ADC?
- What is a successive approximation ADC?
- What is an algorithmic ADC?
- What is a flash ADC?
- What is a pipelined ADC?
- What are the pros and cons of the Nyquist-rate ADCs?

Nyquist-Rate ADCs

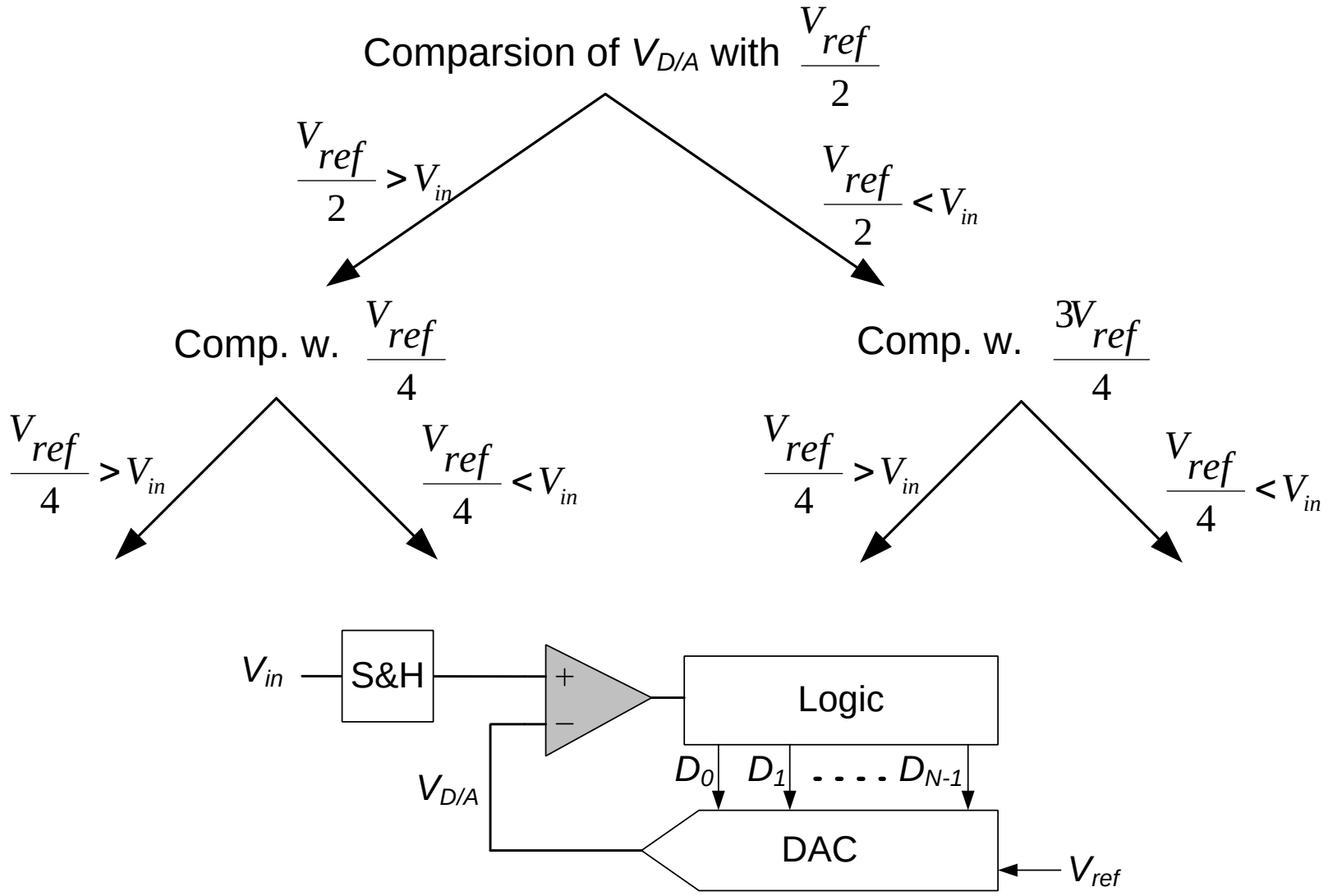
- Sampling frequency f_{samp} is in the same range as frequency f_{in} of input signal
- Low-to-medium speed and high accuracy ADCs
  - Integrating
- Medium speed and medium accuracy ADCs
  - Successive Approximation
  - Algorithmic
- High speed and low-to-medium accuracy ADCs
  - Flash
  - Two-Level Flash
  - Pipelined

Successive Approximation ADC

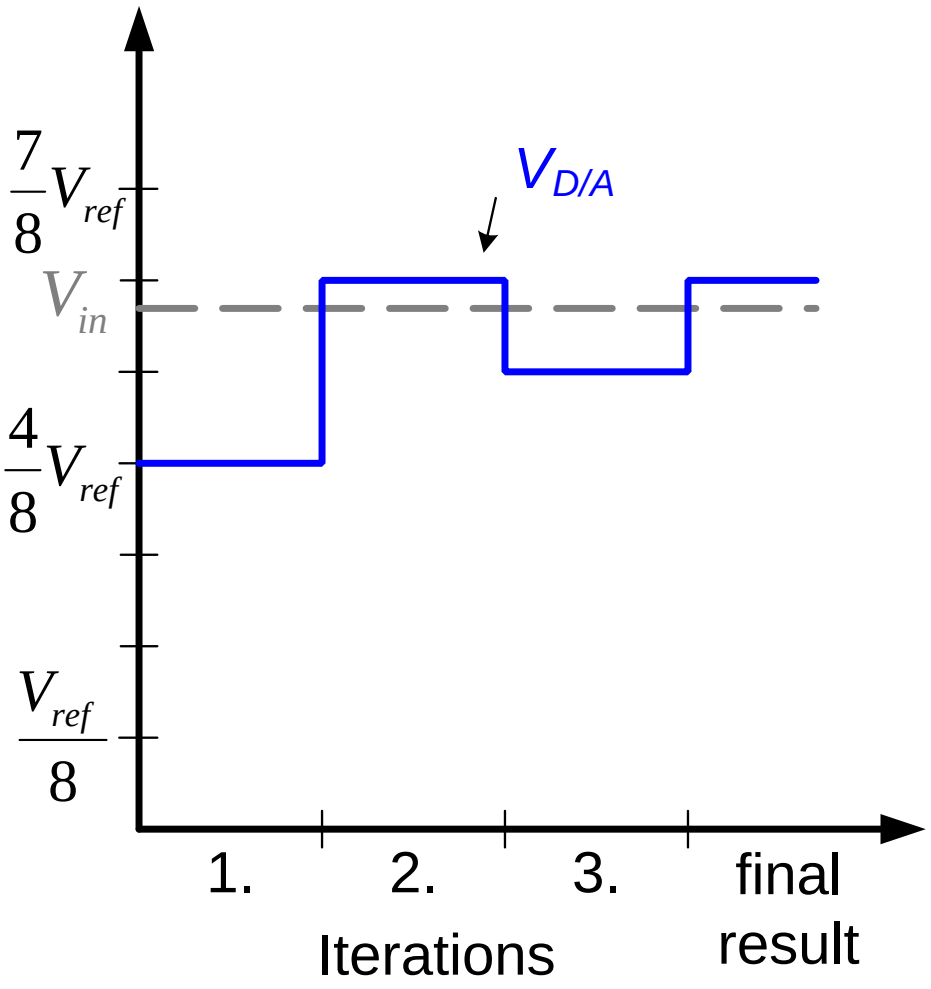
- Generate internal analog signal $V_{D/A}$
- Compare $V_{D/A}$ with input signal V_{in}
- Modify $V_{D/A}$ by $D_0D_1D_2\ldots D_{N-1}$ until closest possible value to V_{in} is reached

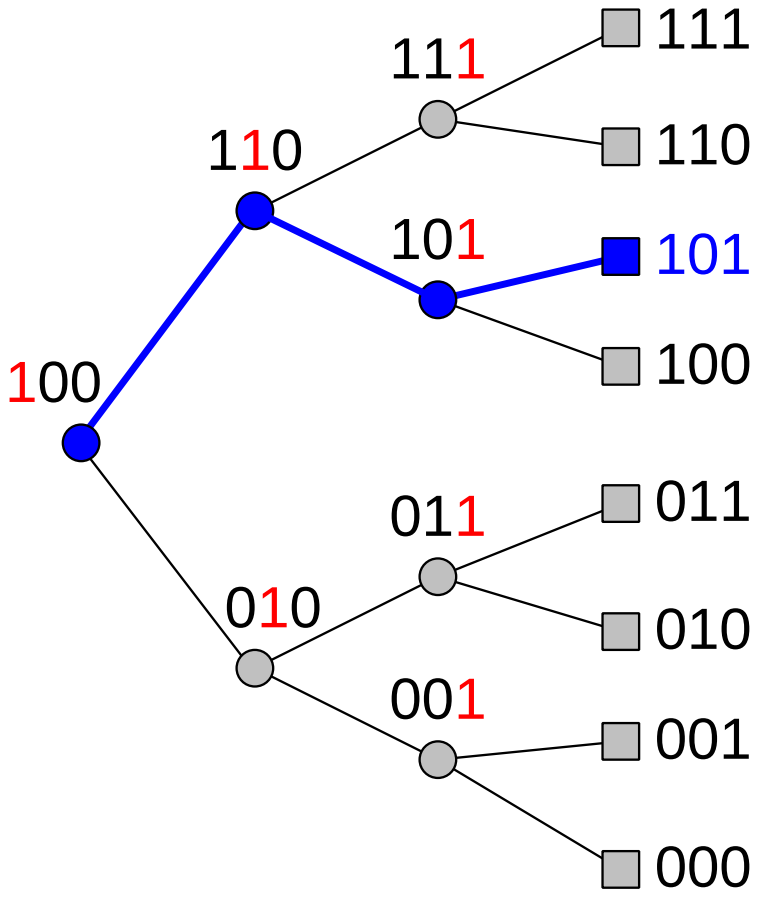


Successive Approximation ADC cont'd



Successive Approximation ADC cont'd





P. Fischer, *VLSI-Design - ADC und DAC*, Uni Mannheim, 2005

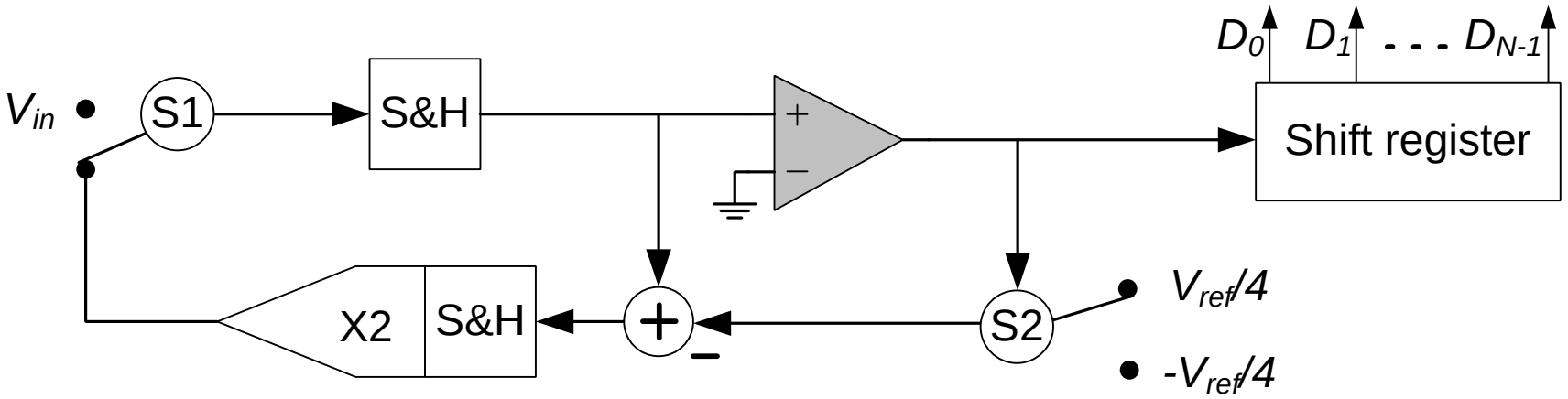
Successive Approx.: pros and cons

- ✓ Low Area / Low Power

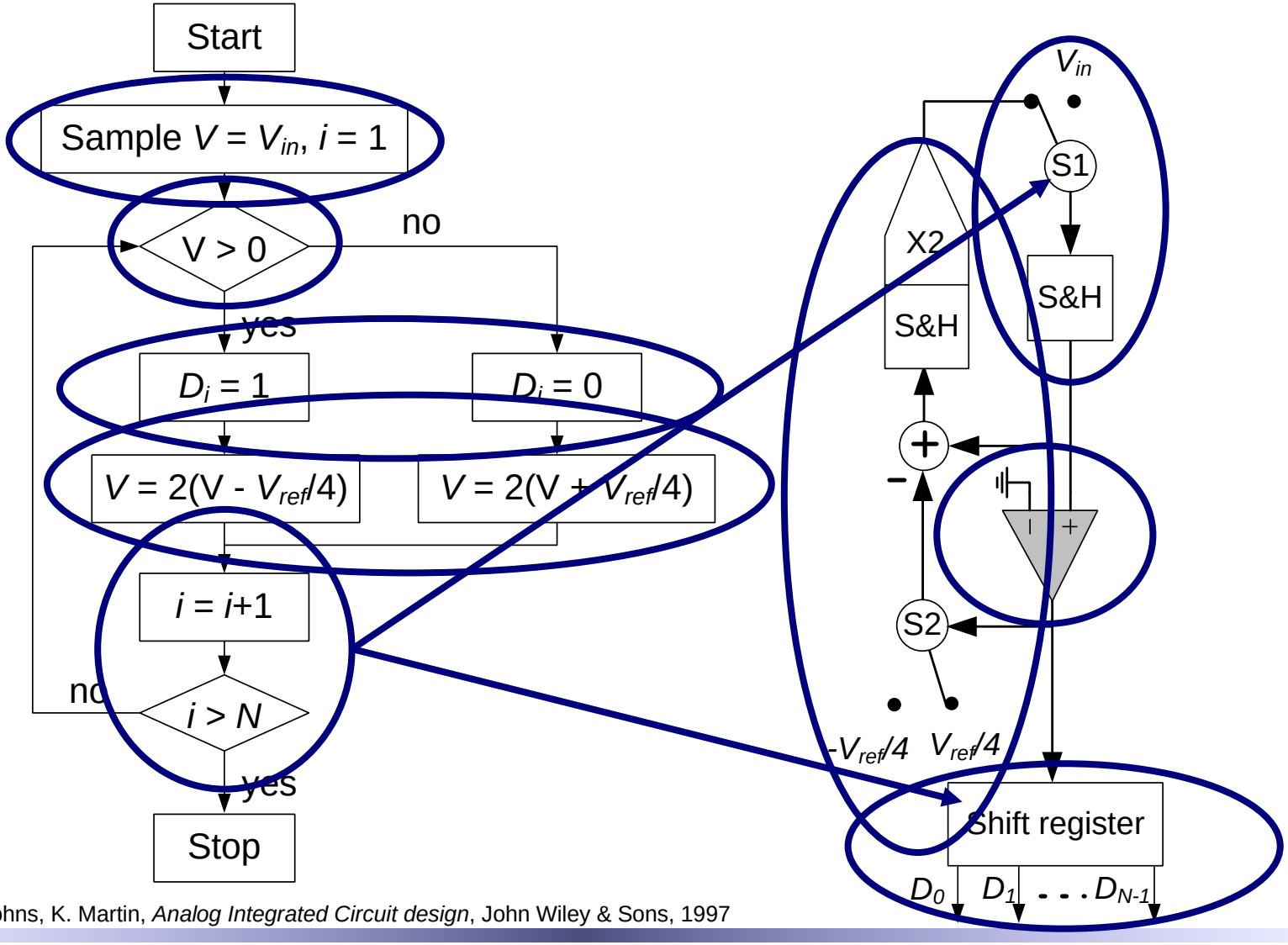
- ✘ High effort for DAC
- ✘ Early wrong decision leads to false result

Algorithmic ADC

- Same idea as successive approximation ADC
- Instead of modifying V_{ref} → doubling of error voltage (V_{ref} stays constant)



Algorithmic ADC con't



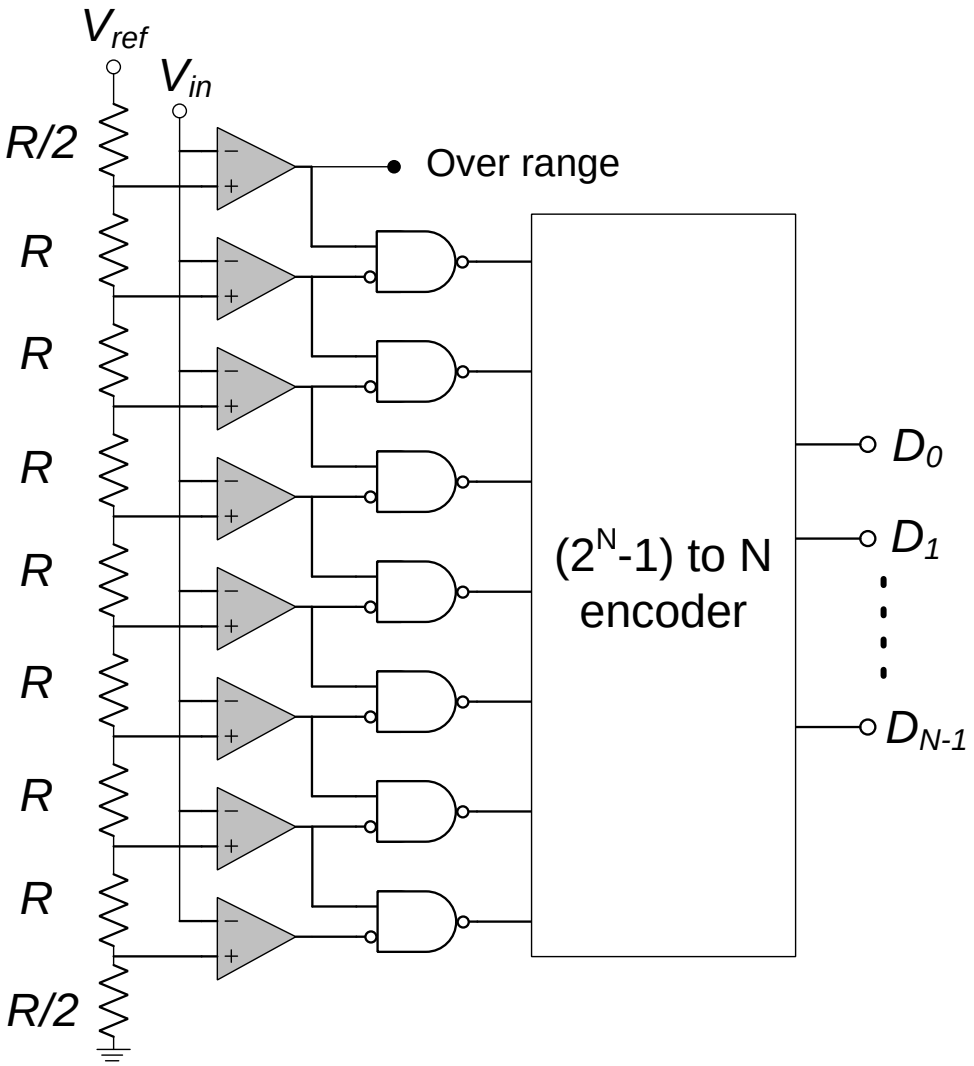
D.A.. Johns, K. Martin, *Analog Integrated Circuit design*, John Wiley & Sons, 1997

Algorithmic ADC: pros and cons

- ✓ Less analog circuitry than Succ. Approx. ADC
- ✓ Low Power / Low Area

- ✘ High effort for multiply-by-two gain amp

Flash ADC



- V_{in} connected with 2^N comparators in parallel
- Comparators connected to resistor string
- Thermometer code
- $R/2$-resistors on bottom and top for 0.5 LSB offset

Some Flash ADC design issues

- Input capacitive loading on V_{in}
- Switching noise if comparators switch at the same time
- Resistors-string bowing by input currents of bipolar comparators (if used)
- Bubble errors in the thermometer code based on comparator's metastability

Flash ADC: pros and cons

✓ Very fast

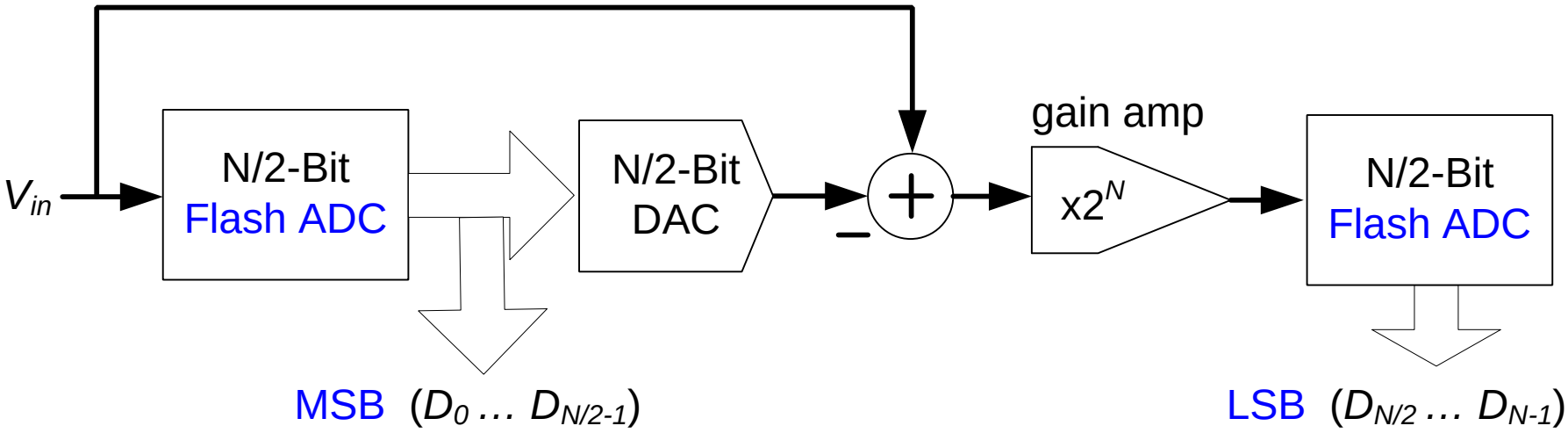
✘ High effort for the 2^N comparators

✘ High Area / High Power

➥ Recommended for 6-8 Bit and less

Two-Level Flash ADC

- Conversion in two steps:
  1. Determination of MSB-Bits and reconverting of digital signal by DAC
  2. Subtraction from V_{in} and determination of LSB-Bits
- F.e. 8-Bit-ADC: Flash: 2^8=256 comparators, Two-level: $2 \cdot 2^4$ = 32 comparators



Two-Level Flash ADC: pros and cons

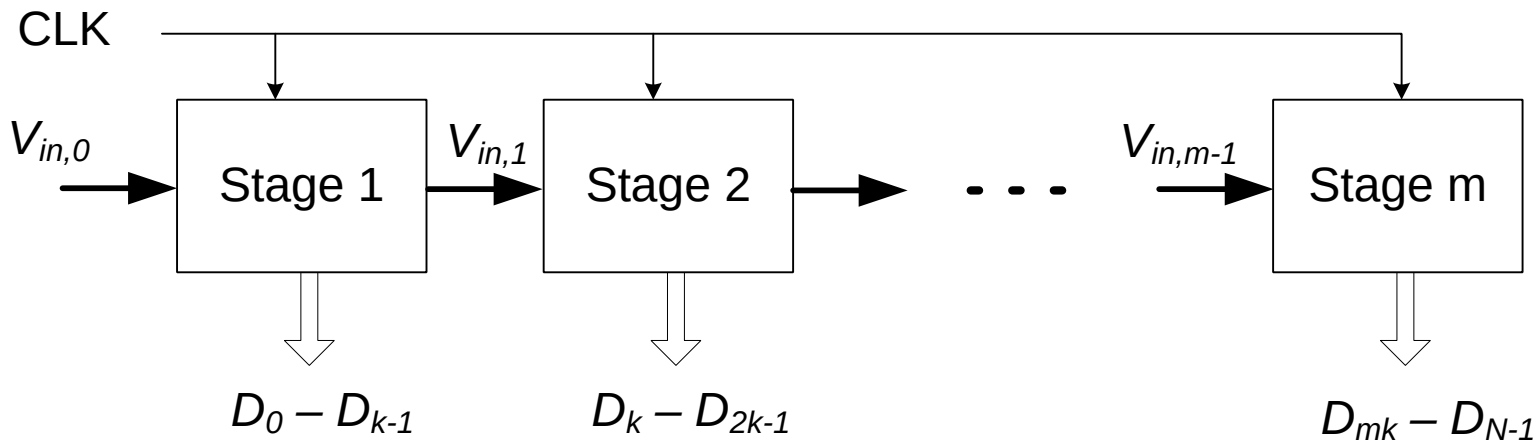
- ✓ Same throughput as Flash ADC
- ✓ Less area, less power, less capacity loading than Flash ADC
- ✓ Easy error-correction after first stage

- ✘ Larger latency delay than Flash ADC
- ✘ Design of *N*/2-Bit-DAC

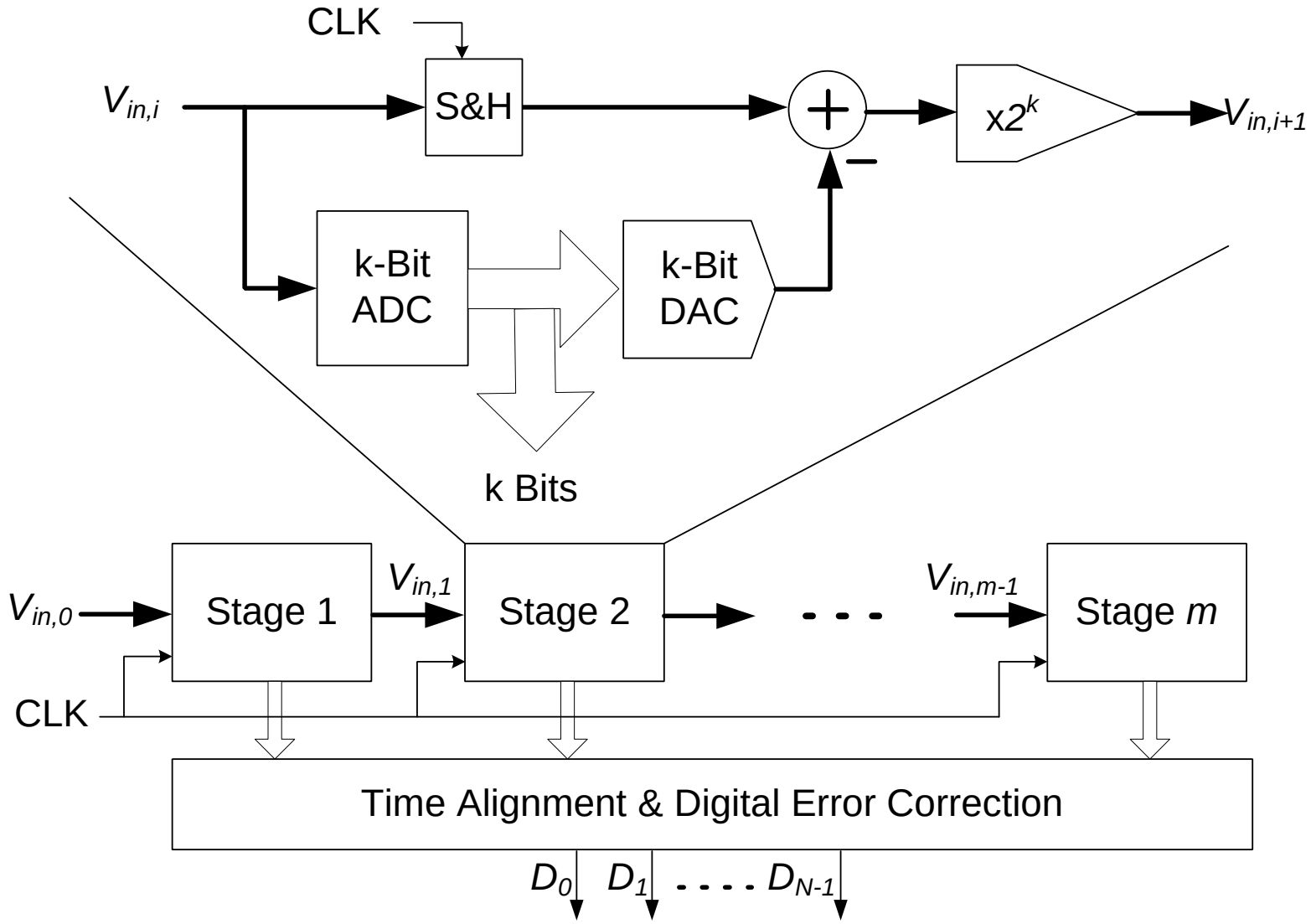
- ➥ Currently most popular approach for high-speed/medium accuracy ADCs

Pipelined ADCs

- Extension of two-level architecture to multiple stages (up-to 1 Bit per stage)
- Each stage is connected with CLK-signal
  - ↳ Pipelined conversion of subsequent input signals
  - ↳ First result after *m* CLK cycles (*m* - amount of stages)
- Stages can be different



Pipelined ADCs: Scheme



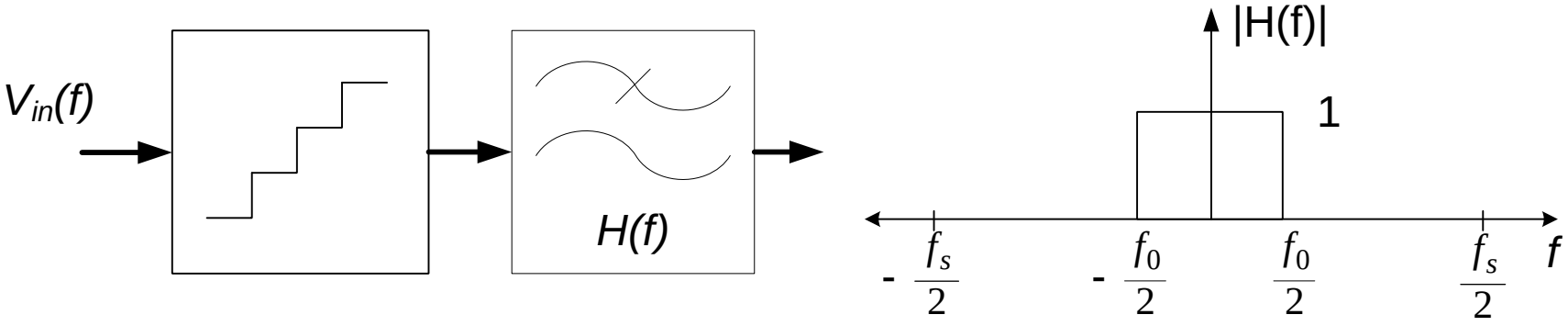
Pipelined ADC: pros and cons

- ✓ High throughput
- ✓ Easy upgrade to higher resolutions

- ✘ High demands on speed and accuracy on gain amplifier
- ✘ High CLK-frequency needed
- ✘ High Power

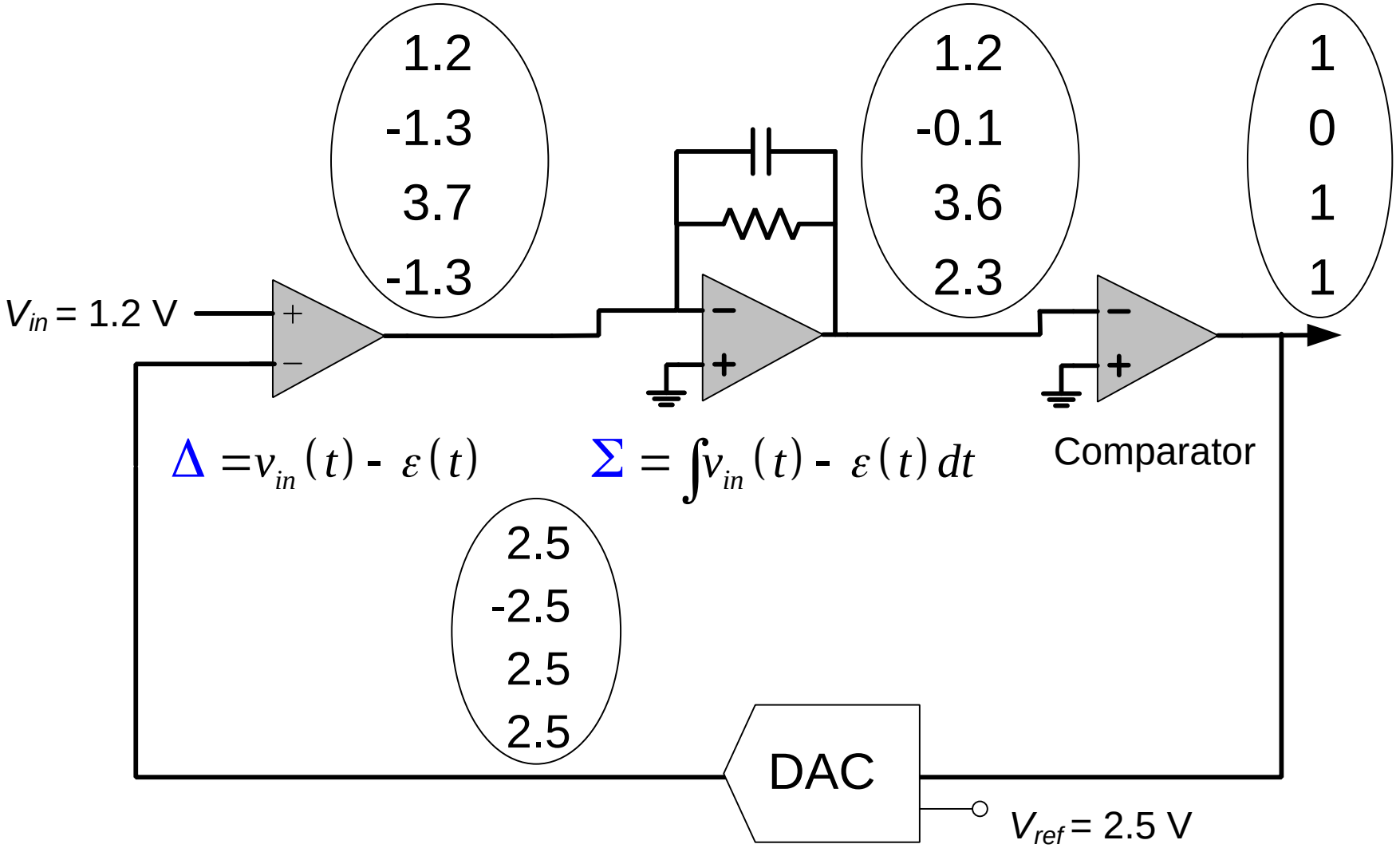
Oversampling (OS)

- Quantized signal is low-pass filtered to frequency f_0
  - elimination of quantization noise greater than f_0

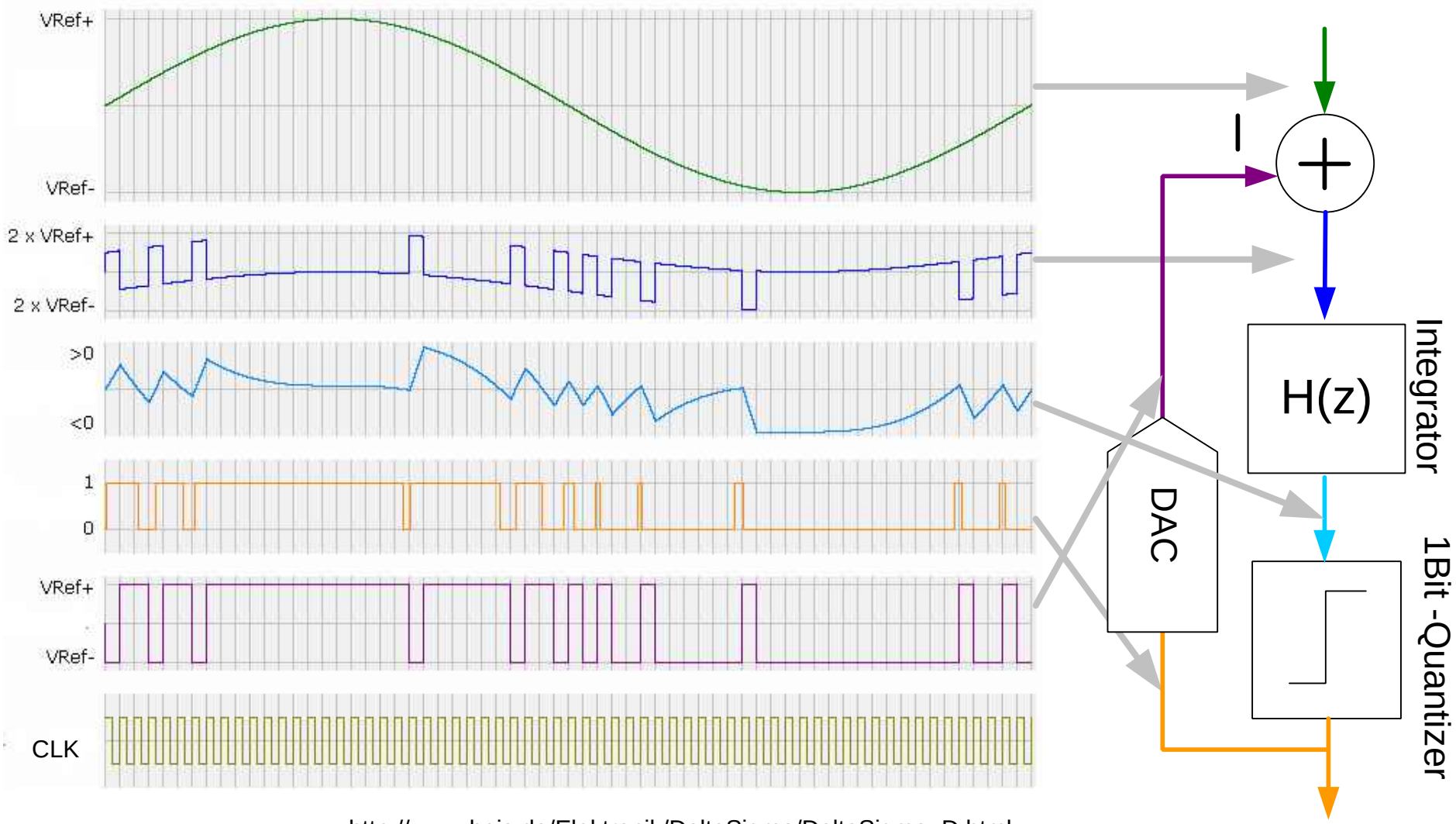


- Oversampling rate (*OSR*) is ratio of sampling frequency f_s to Nyquist rate of f_0
  - $OSR = \frac{f_s}{2 f_0}$

Sigma Delta ADC Example



Sigma Delta ADC Example (Curves)



http://www.beis.de/Elektronik/DeltaSigma/DeltaSigma_D.html

Sigma Delta ADC: pros and cons

- ✓ High resolution
- ✓ Less effort for analog circuitry

- ✘ Low speed
- ✘ High CLK-frequency

➥ Currently popular for audio applications

5. Practical issues

- What are the performance limitations of ADCs?
- What are the differences between PCB- and IC-designs?
- Are there hints to improve the ADC design?
- What are S&H circuits?

Performance Limitations

Analog circuit performance limited by:

- High-frequency behavior of applied components
- Noise
  - Crosstalk (analog ↔ analog, analog ↔ digital)
  - Power supply coupling
  - Thermal noise (white noise)
- Parasitic components (capacitances, inductivities)
- Wire delays

PCB- versus IC-Design

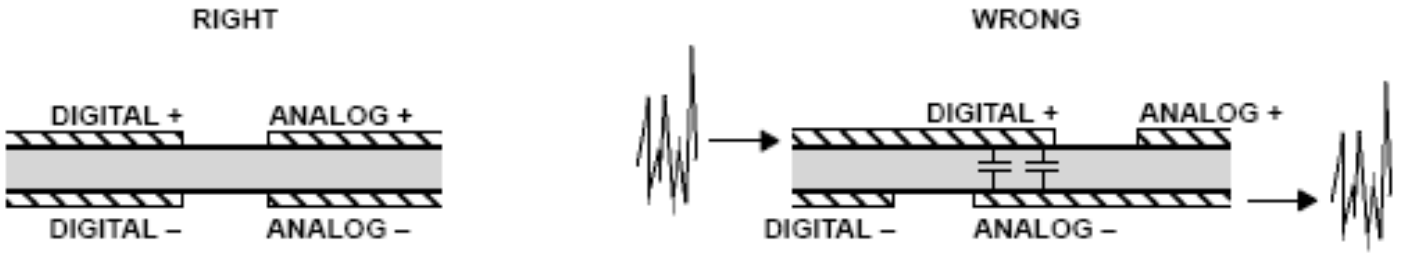
- PCB: Printed Circuit Board, IC: Integrated Circuit
- Noise in PCB-circuits much higher than in ICs
- Influences of parasitics in PCB-circuits much higher than in ICs
- High-frequency behavior of PCB-circuits much worse than of ICs
- Wire delays in PCB much higher than in ICs

↳ *High accuracy, high speed, high bandwidth ADCs only possible in ICs!*

Some Hints for Mixed Signal Designs

For PCB and IC:

- Keep ground lines separate!
- Don’t overlap digital and analog signal wires!

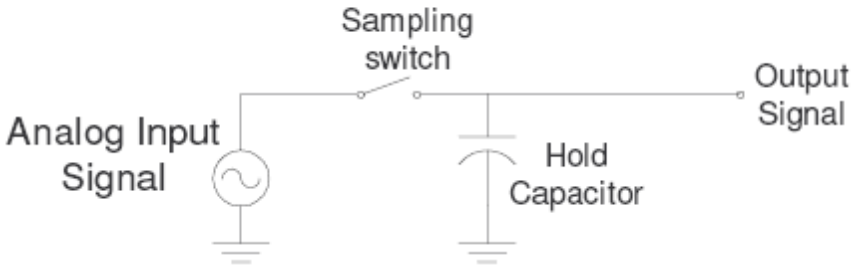


Mancini, *Opamps for everyone*, Texas Instr., 2002

- Don’t overlap digital and analog supply wires!
- Locate analog circuitry as close as possible to the I/O connections!
- Choose right passive components for high-frequency designs! (only PCB)

Sample and Hold Circuits

- S&H circuits hold signal constant for conversion
- A sample and a hold device (mostly switch and capacitor)
- Demands:
  - Small RC-settling-time (voltage over hold capacitor has to be fast stable at < 1 LSB)
  - Exact switching point (else “aperture-error”)
  - Stable voltage over hold capacitor (else “droop error”)
  - No charge injection by the switch



6. Low Power ADC Design

- What are the main components of power dissipation?
- How can each component be reduced?
- What are the differences between power and energy?

Power Dissipation

Two main components:

- Dynamic power dissipation (P_{dyn})
  - Based on circuit's activity
  - Square dependency on supply voltage V_{DD}^2
  - Dependent on clock frequency f_{clk}
  - Dependent on capacitive load C_{load}
  - Dependent on switching probability α

  ↳ $P_{dyn} = V_{DD}^2 \cdot C_{load} \cdot f_{clk} \cdot \alpha$
- Static power dissipation (P_{static})
  - Constant power dissipation even if circuit is inactive
  - Steady low-resistance connections between VDD und GND (only in some circuit technologies like pseudo NMOS)
  - Leakage (critical in technologies ≤ 0.18 µm)

Low Power ADC Design

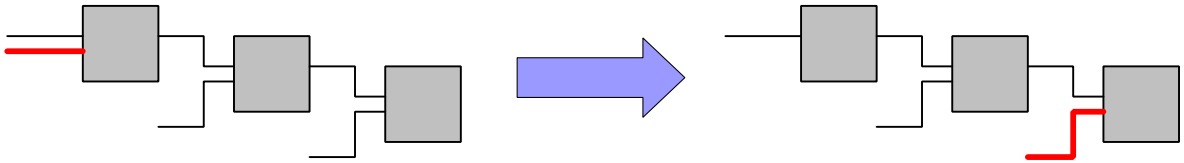
- Reduction of V_{DD}:
  - Highest influence on power ($P \sim V_{DD}^2$)
  - Sadly, delay increases ($t_d \sim 1/V_{DD}$)
  - Sadly, loss of maximal amplitude → SNR goes down
  - Possible solutions:
    - Different supply voltages within the design
    - Dynamic change of V_{DD} depending on required performance
- Reduction of f_{clk}:
  - Dynamic change of f_{clk}

Low Power ADC Design cont'd

- Reduction of C_{load}:
  - C_{load} depends on transistor count and transistor size, wire count and wire length
  - Possible Solutions:
    - Reduction of amount evaluating components
    - Sizing of the design = all transistor get minimum size to reach desired performance
    - Intelligent placing and routing

Low Power ADC Design cont'd

- Reduction of α:
  - Activity = possibility that a signal changes within one clock cycle
  - Possible Solutions:
    - Clock gating → no clock signal to inactive blocks
    - High active signals connected to the end of blocks



    - Asynchronous designs

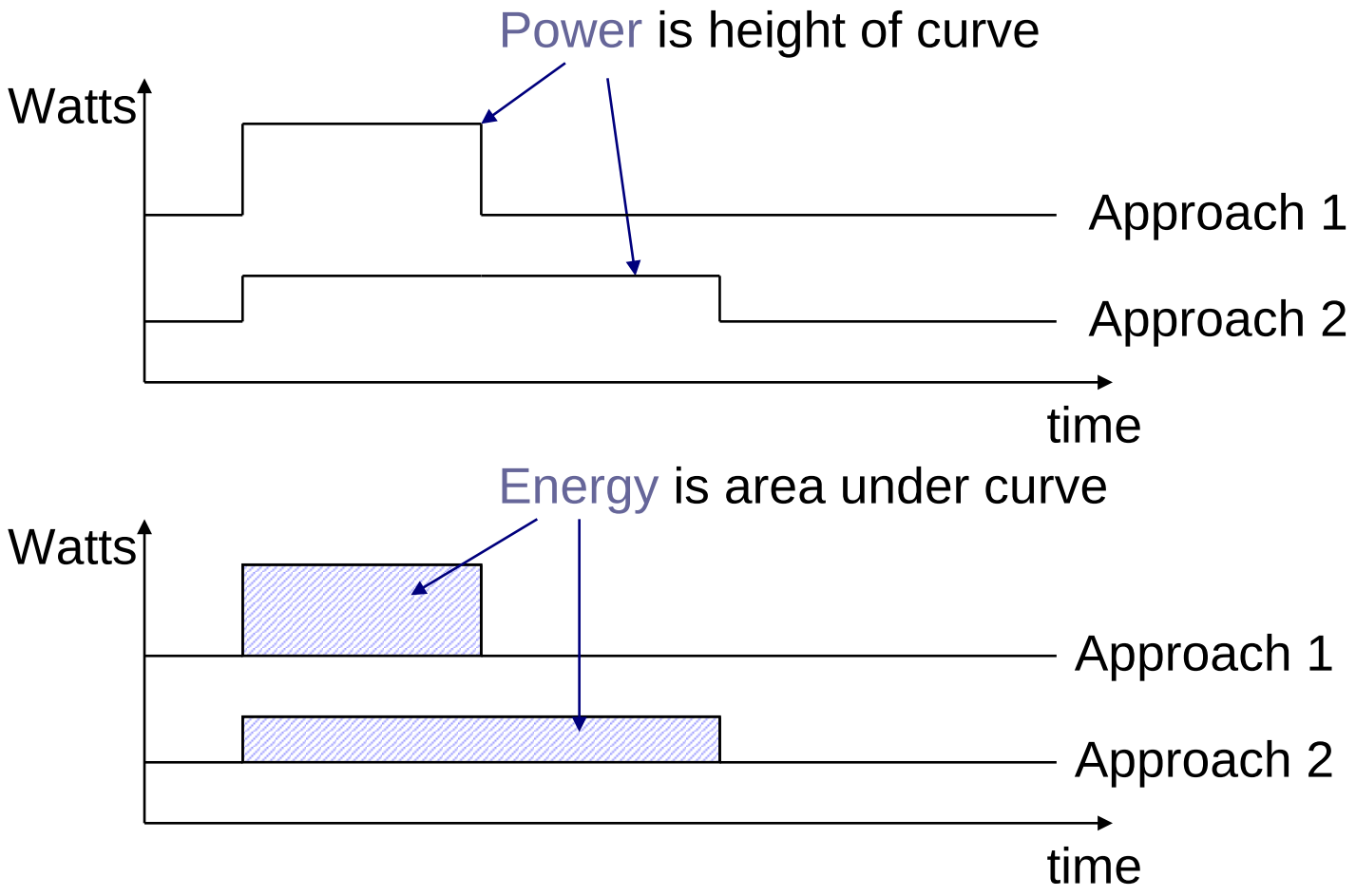
Which ADC for Low Power?

- If low speed: Dual Slope ADC
  - Area is independent of resolution
  - Less components
  - Problem: Counter
- If medium / high speed: mixed solutions
  - Popular: pipelined ADC with SAR
  - Pipelined solutions allows reduction of V_{DD}
  - Long latency but high throughput

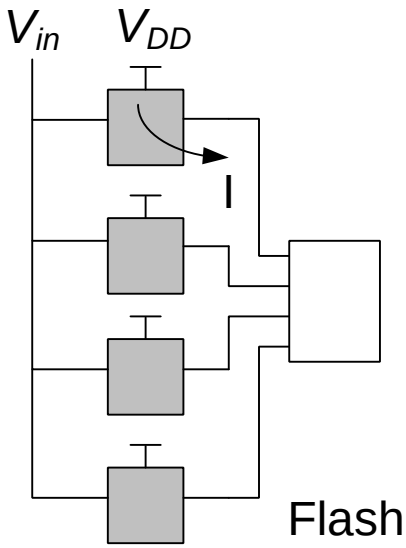
Power vs. Energy

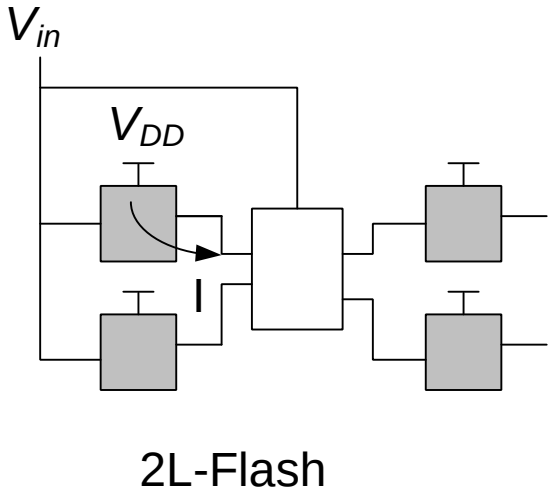
- Power consumption in Watts
  - Power = voltage · current at a specific time point
  - Peak power:
    - Determines power ground wiring designs and Packaging limits
    - Impacts of signal noise margin and reliability analysis
- Energy consumption in Joules
  - Energy = power · delay (joules = watts * seconds)
  - Rate at which power is consumed over time
  - Lower energy number means less power to perform a computation at the same frequency

Power vs. Energy cont'd



Power vs. Energy: Simple Example





- Shaded blocks are ignored
- Dissipation for one input signal:

	V_{DD}	I (each gray block)	Delay	Power	Energy
Flash	1 V	1 µA	1 ns	4 µW	4 fJ
2L-Flash	1 V	1 µA	2.5 ns	2 µW	5 fJ

Low Power ADCs Conclusion

- There is no patent solution for low power ADCs!
- Every solution depends on the specific task.
- Before optimization analyze the problem:
  - Which resolution?
  - Which speed?
  - What are the constraints (area, energy, V_{DD}, V_{in},…)?
  - Which technology can be used?
- Think also about unconventional solutions (dynamic logic, asynchronous designs, …).

Basic ADC Literature

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